Defence Research and Development Canada
Recherche et développement pour la défense Canada

DEFENCE R&D DÉFENSE

Silicon RFIC techniques for reconfigurable military applications

Scott McLelland, Khelifa Hettak, Carole Glaser, Luc DesOrmeaux, Gilbert Morin

Defence R&D Canada – Ottawa
Technical Report
DRDC Ottawa TR 2008-295
December 2008

Canada

Report Documentation Page

Form Approved
OMB No. 0704-0188

1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED
DEC 2008		**00-00-2008 to 00-00-2008**

4. TITLE AND SUBTITLE	5a. CONTRACT NUMBER
Silicon RFIC techniques for reconfigurable military applications	5b. GRANT NUMBER
	5c. PROGRAM ELEMENT NUMBER
6. AUTHOR(S)	5d. PROJECT NUMBER
	5e. TASK NUMBER
	5f. WORK UNIT NUMBER
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) **Defence R&D Canada - Ottawa,3701 Carling Avenue,Ottawa, Ontario K1A 0Z4,**	8. PERFORMING ORGANIZATION REPORT NUMBER
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)	10. SPONSOR/MONITOR'S ACRONYM(S)
	11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution unlimited

13. SUPPLEMENTARY NOTES

14. ABSTRACT

The functionality of silicon radio frequency integrated circuits (RFICs) makes the technology particularly suitable for reconfigurable circuits. Designing silicon RFICs requires expertise in the design, simulation and verification of traditional monolithic microwave integrated circuits (MMICs) while also considering a number of requirements unique to silicon RFIC technology. This report shows how MMIC and RFIC design techniques can be combined to yield high performance circuits and a comprehensive design flow for silicon RFICs. This RFIC design flow was validated by designing both linear and nonlinear circuits that were fabricated using a commercial 0.35-μm SiGe BiCMOS process. These circuits include low noise amplifiers, a voltage controlled oscillator, a double-balanced mixer, a reflection type phase shifter, an analog vector modulator and a 4-bit vector modulator. The two vector modulators generate the variable amplitude and phase weights needed for adaptive phase arrays, which have been proposed to improve the anti-jamming performance of military GPS units.

15. SUBJECT TERMS

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			
unclassified	**unclassified**	**unclassified**	**Same as Report (SAR)**	**174**	

Silicon RFIC techniques for reconfigurable military applications

Scott McLelland, Khelifa Hettak, Carole Glaser, Luc DesOrmeaux
Communications Research Centre Canada

and

Gilbert Morin
Defence R&D Canada - Ottawa

Defence R&D Canada – Ottawa

Technical Report
DRDC Ottawa TR 2008-295
December 2008

Principal Authors

Original signed by Scott McLelland / Khelifa Hettak

Scott McLelland / Khelifa Hettak

Research Engineer / Research Scientist

Approved by

Original signed by Joseph Schlesak

Joseph Schlesak

Manager, Defence Communications Program

Approved for release by

Original signed by Pierre Lavoie

Pierre Lavoie

Chief Scientist, Defence R&D Canada - Ottawa

Abstract

The functionality of silicon radio frequency integrated circuits (RFICs) makes the technology particularly suitable for reconfigurable circuits. Designing silicon RFICs requires expertise in the design, simulation and verification of traditional monolithic microwave integrated circuits (MMICs) while also considering a number of requirements unique to silicon RFIC technology. This report shows how MMIC and RFIC design techniques can be combined to yield high performance circuits and a comprehensive design flow for silicon RFICs. This RFIC design flow was validated by designing both linear and nonlinear circuits that were fabricated using a commercial 0.35-µm SiGe BiCMOS process. These circuits include low noise amplifiers, a voltage controlled oscillator, a double-balanced mixer, a reflection type phase shifter, an analog vector modulator and a 4-bit vector modulator. The two vector modulators generate the variable amplitude and phase weights needed for adaptive phase arrays, which have been proposed to improve the anti-jamming performance of military GPS units.

Résumé

La fonctionnalité des circuits intégrés de radiofréquence en silicium (RFICs) rende la technologie particulièrement appropriée aux circuits re-configurables. Concevoir des RFICs en silicium exige l'expertise dans la conception, la simulation et la vérification des circuits intégrés monolithiques hyperfréquences (MMICs) traditionnels tout en considérant également un certain nombre de conditions uniques à la technologie du RFIC en silicium. Ce rapport met en évidence comment des techniques de conception en MMIC et en RFIC peuvent être conjugués pour générer des circuits a haut rendement et un processus de conception compréhensive pour le RFICs en silicium. Cet processus de conception de RFIC a été validé en concevant les circuits linéaires et non-linéaires qui ont été fabriqués en utilisant un processus commercial 0.35-µm SiGe BiCMOS. Ces circuits incluent des amplificateurs à faible bruit, un oscillateur commandé par une source de tension, un mélangeur double-équilibré, un déphaseur à réflexion, un modulateur vectoriel analog et un modulateur vectoriel à 4 bits. Les deux modulateurs vectoriels produisent des poids variables en amplitude et en phase requis pour les réseaux phasés adaptatifs, qui ont été proposées pour améliorer la performance antibrouillage des unités GPS militaires.

This page intentionally left blank.

Executive summary

Silicon RFIC techniques for reconfigurable military applications

S. R. McLelland; K. Hettak; C. Glaser; L. DesOrmeaux; G. A. Morin; DRDC Ottawa TR 2008-295; Defence R&D Canada – Ottawa; December 2008.

Introduction: Reconfigurable circuits, used in adaptive arrays (smart antennas) and software-defined radios, are perhaps best implemented using silicon radio frequency integrated circuit (RFIC) technology. The performance of silicon RFICs is comparable to, and sometimes better than, traditional gallium arsenide monolithic microwave integrated circuits (GaAs MMICs). Silicon RFICs can be highly integrated and can include mixed analog-digital designs (allowing DSP control of analog functions). Successfully designing silicon RFICs requires knowledge of traditional MMIC design along with additional design techniques specific to silicon technology. Furthermore, the simulation and verification CAD tools for silicon RFICs differ from the design flow used for traditional MMIC design. Therefore, the objectives of this project were to:

investigate silicon-specific RFIC design techniques for reconfigurable military applications,

establish a simulation and verification design flow for silicon RFICs, and

verify the first two objectives by designing and fabricating both linear and nonlinear RFICs (including specific RFICs for military adaptive phased arrays).

Results: Linear and nonlinear RFICs were designed and fabricated using a commercially available 0.35µm SiGe BiCMOS process. These RFICs included cascode low noise amplifiers, a cross-coupled differential oscillator and a Gilbert Cell mixer. Silicon RFICs capable of generating variable weights (both amplitude and phase) for reconfigurable, adaptive phased arrays were also demonstrated. All of the designs addressed limitations unique to silicon RFICs, such as the substrate loss and fabrication design rules specific to analog integrated circuits on silicon. A new simulation and verification design flow for silicon RFICs was also established where Agilent ADS was used for simulation, Mentor Graphics IC Station was used for layout and Mentor Graphics Calibre was used for verification.

Significance: Silicon RFIC techniques, when combined with traditional MMIC design, provide designers with the widest possible range of circuit options to realize high-performance RF front-ends. Silicon RFICs possess unique advantages that may improve RF font-ends, such as: 1) mixed analog-digital designs capable of dynamically reconfiguring a circuit to improve its performance or switch to a different operating mode, and 2) a large number of metal layers that can be exploited by innovative electromagnetic design to reduce the size and loss of the RFIC's passive components. Although silicon RFIC techniques continue to be actively researched, the design flow described in this report can be used to produce RFICs with first-pass design success.

Future plans: The silicon RFIC design techniques developed for this project will be used in a new, multi-year DRDC project on electronics for adaptive-nulling in GPS phased arrays.

Sommaire

Silicon RFIC techniques for reconfigurable military applications

S. R. McLelland; K. Hettak; C. Glaser; L. DesOrmeaux; G. A. Morin; DRDC Ottawa TR 2008-295; R & D pour la défense Canada – Ottawa; Décembre 2008.

Introduction: Les circuits re-configurable, utilisés dans des réseaux adaptatifs (antennes intelligentes) et des radios logicielles, peut-être mieux réalisés en utilisant la technologie du circuit intégré radiofréquence en silicium (RFIC). La performance du RFIC en silicium est comparable à, et parfois meilleur que, les circuits intégrés monolithiques hyperfréquences traditionnelles en arséniure de gallium (GaAs MMICs). RFICs en silicium peut être fortement intégré et peut inclure des conceptions combinées analog-numériques (permettant le contrôle des fonctions analogs par le biais du traitement numérique du signal). Concevoir avec succès le RFICs en silicium exige la connaissance de la conception MMIC traditionnelle combiné à des techniques de conception additionnelles spécifiques à la technologie silicium. En outre, la simulation et les outils de vérification CAO (Conception Assistée par Ordinateur) pour RFICs en silicium diffèrent du processus de conception utilisé pour la conception de MMIC traditionnelle. Par conséquent, les objectifs de ce projet étaient:

Investiguer les techniques de conception RFIC en silicium spécifiques pour des applications militaires re-configurables,

Établir les méthodologies pour effectuer les simulations et les vérifications du cycle de conception pour le RFICs en silicium, et

Vérifiez les deux premiers objectifs en concevant et en fabriquant les deux RFICs linéaire et non-linéaire (y compris les RFICs spécifiques pour les réseaux phasé militaires adaptatifs).

Résultats: Les circuits RFICs linéaire et non-linéaire ont été conçus et fabriqués en utilisant un processus commercial 0.35µm SiGe BiCMOS. Ces RFICs incluent des amplificateurs de type cascode à faible bruit, un oscillateur différentiel de type couplage en croix et un mélangeur de type cellule de Gilbert. Le RFICs en silicium capable de produire des poids variables (simultanément amplitude et phase) pour la reconfiguration, et réseaux phasés adaptatives ont été également démontrés. Toutes les conceptions ont adressé les limitations uniques au RFICs en silicium, tel que les pertes due au substrat et les règles de conception de fabrication spécifique aux circuits intégrés analogs sur le silicium. Une nouvelle approche de simulation et vérification du processus de conception pour le RFICs en silicium a été également établie où le logiciel Agilent ADS a été utilisé pour la simulation, la station d'IC de Mentor Graphics a été utilisée pour le graphique et le logiciel Calibre de Mentor Graphics a été utilisé pour la vérification.

Importance: Les techniques de RFICs de silicium, une fois combinées avec la conception MMIC traditionnelle, fournissent aux concepteurs le plus grand choix possible des options pour la réalisation de circuit inhérent au premier étage transmetteur RF à rendement élevées. RFICs en silicium possèdent les avantages uniques qui peuvent améliorer le premier étage transmetteur RF, comme: 1) conceptions combinées analog–numérique capables de reconfigurer dynamiquement un circuit pour améliorer sa performance ou commuter à un mode d'opération différent, et 2) un grand nombre de couches en métal qui peuvent être exploitées par une conception

électromagnétique innovatrice pour réduire la taille et les pertes des composants RFIC passifs. Bien que des techniques du RFIC en silicium continuent à être activement recherchées, le processus de conception décrit dans ce rapport peut être utilisé pour produire RFICs avec un succès de conception dés le premier coup.

Perspectives: Les techniques de conception pour RFIC en silicium développées pour ce projet seront utilisées dans un nouveau RDDC projet à multiple années sur l'électronique pour les réseaux phasés adaptatifs antibrouillage au GPS.

This page intentionally left blank.

Table of contents

List of figures

List of tables

This page intentionally left blank.

1 Introduction

Silicon-based radio frequency integrated circuits (RFICs) offer a number of unique advantages compared with traditional gallium arsenide (GaAs) monolithic microwave integrated circuits (MMICs). Some of these advantages include aggressive analog component scaling (higher inductance/capacitance per unit area), mixed analog and digital designs, and integrated microelectromechanical systems (MEMS). These advantages result in cost savings, improved performance and new functionality at frequencies comparable to traditional GaAs MMICs.

Silicon RFIC design is, however, quite different from traditional GaAs MMIC design. The silicon substrates used have more loss than GaAs wafers and hence designing all types of high-performance passive structures, from inductors to transmission lines, is challenging. Furthermore, there are a number of silicon-specific design requirements, such as metal density, stress and antenna design rules, that impact circuit design and performance. The computer-aided design (CAD) tools are also different from those used for GaAs MMICs, especially for layout and verification. Finally, the silicon RFIC circuit topologies often differ from GaAs MMIC topologies.

Therefore, the goal of this project was to investigate and learn the silicon RFIC design techniques required to successfully exploit the advantages of the technology. This was accomplished by designing three 5×5 mm silicon RFIC wafer tiles that were fabricated and measured. Of the silicon RFIC technologies that are commercially available, silicon germanium (SiGe) heterojunction bipolar transistors (HBTs) are capable of much better performance than comparably sized CMOS devices. Hence, SiGe HBTs were chosen for this project.

The first of the three 5×5 mm wafer tiles, shown in Figure 1, concentrated on linear circuit designs, lumped elements, transmission lines and other passive structures. This first run also focused on learning the new CAD tools required for layout and verification.

The second of the three 5×5 mm wafer tiles, shown in Figure 2, built on the expertise gained from the first run. More complicated, non-linear circuit designs were included along with new passive test structures. Layout versus schematic (LVS) verification software was also used for the first time.

The third of the three 5×5 mm wafer tiles, shown in Figure 3, combined all of the RFIC techniques learned from the first two runs to produce prototype circuitry for adaptive phased arrays, thus demonstrating the capability to design silicon RFICs for future military applications.

This report is organized as follows. First, Chapter 2 describes establishing a silicon RFIC design flow. This design flow includes the choosing and setting up the required CAD tools along with learning the RFIC-specific foundry design rules and techniques. This flow was expanded and improved with each successive tape-out.

With the design flow established, RFICs could be successfully designed, simulated, laid-out and submitted to the foundry for fabrication. Linear circuits were designed first, followed by more complicated non-linear circuits. The linear RFICs are presented in Chapter 3 and include two types of low-noise amplifiers (LNAs): a lumped cascode operating at 5 GHz and a distributed

cascode operating at 20 GHz. The non-linear RFICs are presented in Chapter 4 and include a voltage-controlled oscillator (VCO) and a Gilbert Cell mixer, both operating at 5 GHz.

The RFICs included in Chapters 3 and 4 are fundamental "building-block" linear and non-linear RFICs, whereas Chapter 5 builds upon this expertise by presenting more sophisticated RFICs intended for a specific reconfigurable military application. This application was chosen to be adaptive antennas and Chapter 5 presents designs of a 1.2 GHz 4-bit vector modulator and a 5 GHz analog vector modulator, with the latter including a variable gain amplifier and phase shifters.

Finally, the conclusions and key points resulting from the project are presented in Chapter 6.

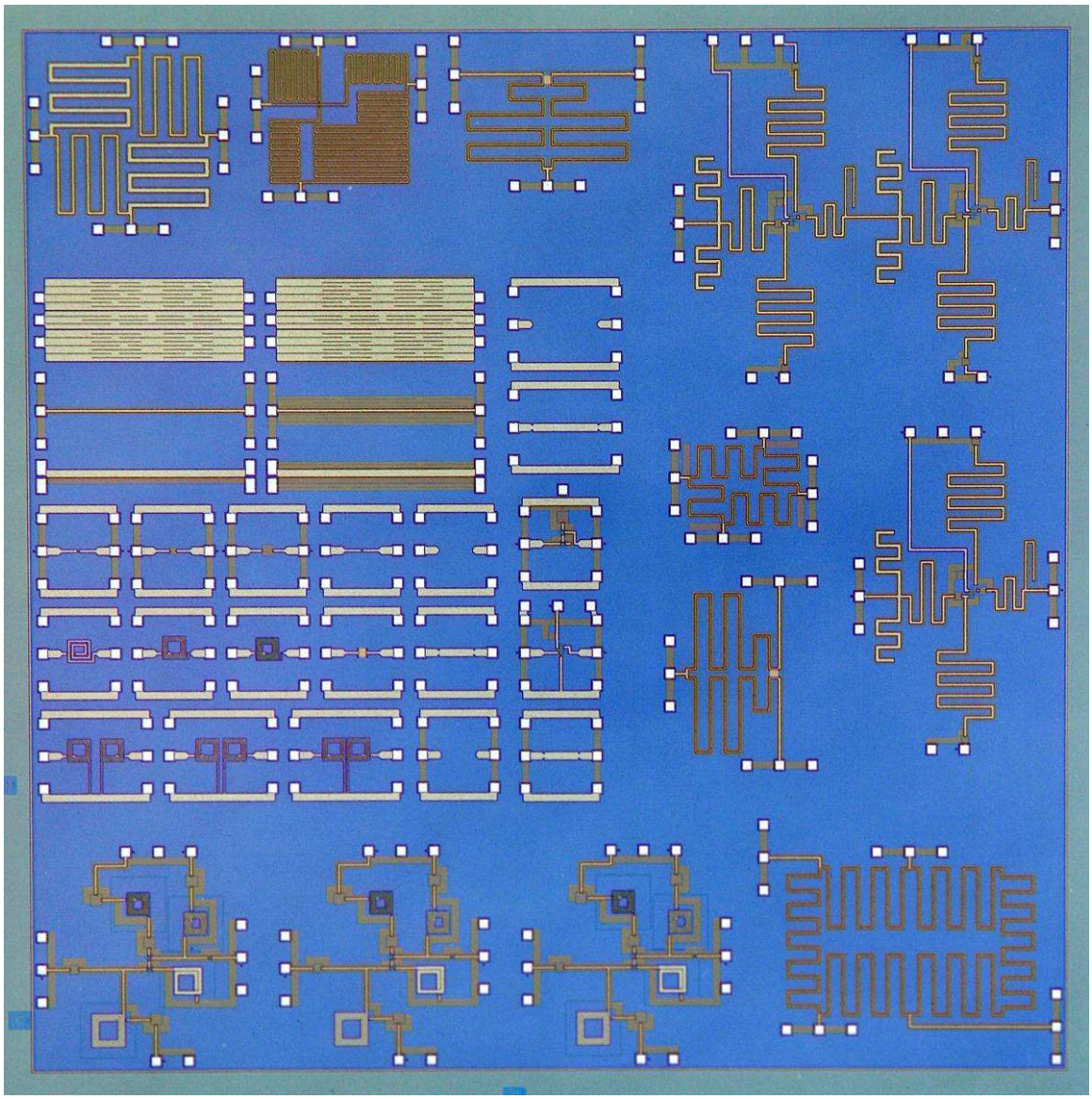


Figure 1: Photograph of the 5×5 mm tile containing linear RFICs

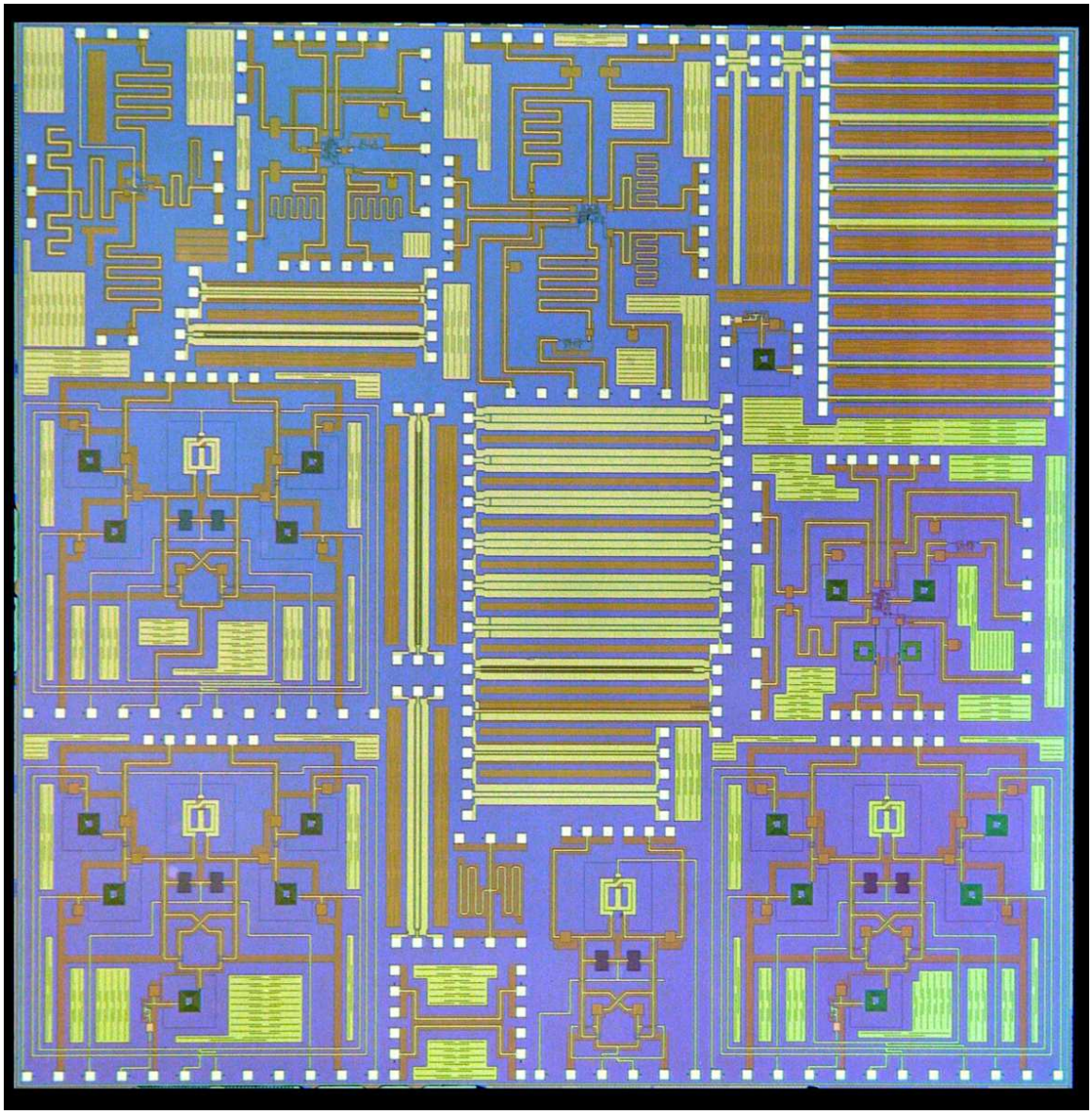


Figure 2: Photograph of the 5×5 mm tile containing nonlinear RFICs

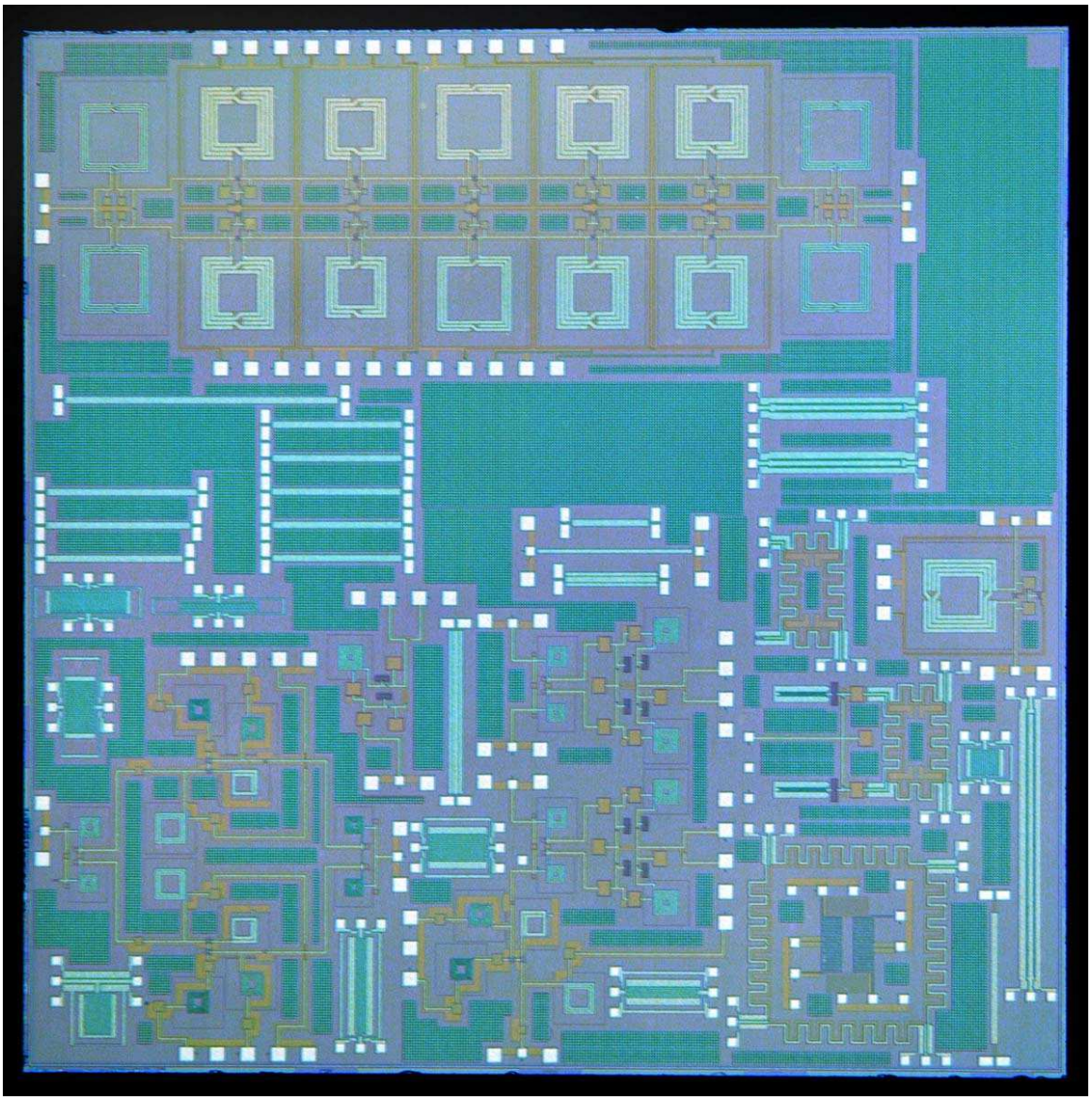


Figure 3: Photograph of the 5×5 mm tile containing RFICs for adaptive phased arrays

2 RFIC Design Flow

2.1 2005 Tape-Out

The 2005 design submission, known as a "tape-out", was our first experience working with a silicon RFIC process and also with the foundry. These facts necessitated learning new software tools and design requirements unique to silicon-based integrated circuits and therefore significant training was required.

The most common flow for the design, layout and verification of SiGe integrated circuits uses the same software, such as Cadence, for all steps. This software suite is, however, extremely expensive and beyond the resources of this project to buy. Accordingly, Agilent ADS was used for circuit design and simulation, ICedit for layout and Mentor Graphics Calibre for design rule checking and verification. In this design flow, only Calibre needed to be purchased. Although Mentor Graphics IC Station could have been used for the layout, our expertise was with ICedit, and hence it was chosen to minimize the amount of training required to successfully lay out the first tape-out.

Unix-based Mentor Graphics IC Station was used to generate layout artwork (pcells) from the foundry design kit, however these pcells were transferred to the PC-based ICedit in gdsii format and used to layout the complete circuits in ICedit. Once the layout was complete in ICedit, gdsii files were again used to transfer the layouts of each individual circuit and then eventually the complete 5×5 mm tile to Mentor Graphics Calibre for error checking using the foundry design kit rules.

Tape-out verification requirements specified by the foundry included error-free data including design rule checking (DRC), which we are familiar with, but also additional checks for stress rules, metal density rules, electrostatic discharge (ESD) rules, latch-up (LUP) rules, electrical rule checking (ERC), and antenna rules. Extra time and assistance from both Mentor Graphics and the foundry support engineers, was used to get the Calibre verification software loaded and working properly, as well as understanding how to complete the rule checks and clear the errors.

Some aspects of the layout, including pads, vias and interconnects, were generated without using the foundry pcell library. These were created manually in ICedit, and as a consequence, Calibre did not recognize these parts of the layout and thus generated some errors. These errors were waived because they were solely a software problem getting Calibre to recognize the custom-drawn elements and the layouts were simply checked manually to verify their correctness. Additionally, some of these errors were warnings that did not apply to our particular circuits.

Of particular note are the Stress and Antenna design rules. These requirements are unique to silicon RFICs and, after time invested to understand the implications of these rules, every circuit layout was modified to comply with these requirements. In some instances these changes required re-simulation and adjustment of the circuits.

Metal Density rules were not enforced by the foundry in 2005 and hence were not applicable to the 2005 tape-out. The 2006 tape-out, however, was subject to this rule and those layouts were affected accordingly.

Layout Versus Schematic (LVS) was not performed on the 2005 tape-out because we did not own the necessary licenses for that function of Calibre at that time. These licenses were, however, purchased prior to the 2006 tape-out. LVS is a very important tool for error checking but not mandatory for the 2005 tape-out.

2.2 2006 Tape-Out

The requirements for the 2006 tape-out again included error-free data for DRC, Stress, ESD/LUP, ERC, and Antenna design rules. An additional error check for minimum Metal Density was added by the foundry in 2006 and meeting this required extra time to add metal fill around all of the individual circuits over the entire 5×5 mm tile. This fill metal must be included on each metal level virtually everywhere across the tile to meet the foundry metal density requirements, however, the metal fill must also not affect the electrical performance of the circuits. Accordingly, the metal fill was added manually to meet both of these requirements simultaneously. Circuit performance was not re-simulated after adding the fill since the fill was added throughout the tile in locations far-enough away from the circuits so as to not affect their performance.

Before the 2006 tape-out the Mentor Graphics software was upgraded to include Design Architect IC which allowed the use of the layout versus schematic (LVS) component of Calibre. This allowed the netlist of an Agilent ADS schematic (used for simulation) to be compared to a netlist generated from the corresponding layout in Mentor Graphics IC Station. LVS confirms that the layout, and hence the fabricated circuit, is identical to the schematic. This comparison is extremely useful because the schematic has been demonstrated through numerous simulations to produce the desired electrical performance.

Extra time and assistance from Mentor Graphics and the foundry support engineers was required to set up and run the LVS software. LVS between two netlists, each generated using two different foundry libraries (one from ADS and one from ICstation), proved to be somewhat difficult since the syntax of the element parameters differed between the two netlists. A significant amount of effort was required to manually adjust the netlists so that LVS could be successfully carried out. In the end, however, this was extremely useful to detect errors between the original design schematics and the final layout, all of which were corrected before submitting the layout for fabrication.

After completion of the 2006 tape-out, several designers and layout staff attended a comprehensive 4-day Mentor Graphics course which included:

project management in ICstudio,

netlist-driven layout and polygon editing in IC Station,

routing and short-checking,

layout verification with Calibre and Inline DRC,

Calibre LVS basics,

texting and connectivity for Calibre LVS,

finding shorts and opens with Calibre LVS, and

Calibre LVS device recognition.

2.3 2007 Tape-Out

"Schematic driven layout" was evaluated for the first time using the 4-bit vector modulator included in the 2007 tape-out. For runs in 2005 and 2006, the foundry design kit was used in Mentor Graphics to generate the layout artwork (pcells) for each of the lumped elements and transistors. These elements were generated individually and then transferred via gdsii format to ICedit for layout. All interconnecting lines between the elements imported from Mentor Graphics were then drawn by hand in ICedit, as were any required vias between metal layers.

While this methodology was successfully used to layout the 2005, 2006 and the majority of the 2007 circuits, it is very labour-intensive. Therefore, to investigate a potential alternative, schematic driven layout was used for the 4-bit vector modulator designed in 2007. Rather than generating the layout pcells for the 4-bit vector modulator individually, the schematic for the 4-bit vector modulator was entered into Mentor Graphics. Calibre was then used to generate the layout of each lumped element and transistor from the parameters contained in the corresponding schematic symbols. This is extremely advantageous because although Calibre generates the same layout artwork that could be produced by manually selecting the element from the foundry library, when the layout is generated from the information in the schematic Calibre retains information about the connectivity between the elements in addition to the element parameters themselves.

Once Calibre has generated the layout pcells for each element, with the connectivity also shown using "ribbons" between the elements, the circuit may be floorplanned. With the connectivity between elements known, placing the elements in the correct position relative to one another is much easier, and potentially less prone to error, compared with doing the same task without the ribbons.

Mentor Graphics can translate these ribbons into actual interconnects with vias, however, the default settings for these interconnects were not appropriate for the microwave circuit designs. Nevertheless, the ribbons represent the locations of the interconnecting lines and so foundry pcells for metal layer vias were generated manually using the foundry design kit and placed at either end of each ribbon where needed to connect from a given element to the metal layer to be used for the interconnect.

The floorplanned layout was then moved to Agilent ADS and the interconnecting microstrip lines were added manually. Since Agilent ADS is specifically designed for microwave circuits, it includes many convenient features to easily add these microstrip lines to the layout. The completed layout was then moved back to Mentor Graphics via gdsii format and Calibre was used to run the design rule checking required for tape-out.

Since schematic driven layout automatically generates all the element layouts, and foundry via pcells were placed using the connectivity "ribbons" from the schematic driven layout, the only manual layout required is the interconnecting microstrip. This means that only a few foundry design rules need to be heeded (those affecting the microstrip lines) and not those that affect the other elements (since these elements are directly from the design kit and are pre-verified by the foundry). Herein lies the distinct advantage of using this approach – *when the completed layout for the 4-bit vector modulator was design rule checked for the first time there were far fewer errors to be corrected.* Using schematic driven layout, along with ribbons and foundry via pcells, inherently forces the majority of the layout to automatically follow the foundry design rules, which of course results in a lower number of violations when the layout is design rule checked for the first time. Furthermore, initial floorplanning using the "ribbon" connectivity between the elements vastly simplifies determining their correct placement and, perhaps more importantly, dramatically reduces the possibility that elements get incorrectly connected, which the design rule checking may not catch. Layout versus schematic may detect this type of error; however, it is still more desirable to avoid it in the first place using the connectivity ribbons.

As with the 2006 run, the 2007 tape-out also required metal fill. For the 2007 run, however, a different fill pattern was used. Small squares, the size of which was specified by the foundry, were used to create an array of fill on all four metal levels. The spacing between the squares in the array was also specified by the foundry.

This type of metal fill proved to be far easier to use for two reasons. First, the array size/spacing was specified by the foundry and was therefore guaranteed to pass design rule checking. Second, the array of small squares was easily inserted into arbitrarily-shaped spaces between the circuits because the array of small squares can 'snake' in the spaces between circuits and, as long as the size and spacing of the squares within the array are respected, the metal fill passes the design rules despite the arbitrary overall shape of the metal fill array.

3 Linear RFICs

3.1 Lumped Cascode LNA at 5 GHz

3.1.1 Introduction

This section describes the design and measured performance of a 5 GHz low noise amplifier (LNA) fabricated using a 0.35 µm silicon germanium (SiGe) hetrojunction bipolar transistor (HBT) process. A lumped element, cascode configuration was chosen with target specifications of:

Noise figure (NF) < 2.5 dB,

$|S_{21}|$ 15 dB

$|S_{22}|$, $|S_{11}|$ < -15 dB

The operating frequency of 5 GHz was arbitrarily chosen and linearity was not addressed (since the goal was to explore linear RFIC design). The LNA design was simulated in Agilent ADS, laid out in Mentor Graphics IC Station and verified using Mentor Graphics Calibre. The tape-out was Dec. 6, 2005.

The LNA design was intended to explore issues specifically related to RFIC design on silicon. These issues include:

Transmission line and via modeling without parasitic extraction

Placement and effects of substrate contacts/ties and guard rings

Proximity of interconnect ground plane to lumped elements (since the lumped element models in ADS assume no ground plane)

Proper spacing of lumped elements/interconnects/transistors for no coupling (models in ADS assume no coupling)

Use of a "substrate" node required by the foundry models

Accuracy of the foundry ADS models

Use of diodes to satisfy antenna design rule checking (DRC)

3.1.2 Cascode Configuration

The classic cascode configuration was chosen for the LNA. A cascode amplifier is a common emitter (CE) stage followed by a common base (CB) stage. There is no interstage matching between the CE stage and the CB stage and this is the key advantage of the cascode amplifier.

The CE stage suffers from the Miller multiplier effect (the CB stage does not), but the cascode reduces this Miller effect. The collector of the CE stage is fed into the emitter of the CB stage, with no interstage matching, thus the load resistance of the CE stage is the input resistance (r_e or

$1/g_m$) of the CB stage. The mismatch of presenting this low load resistance (r_e) reduces the Miller multiplier effect of $C_{\mu 1}$ and thus extends the upper cut-off frequency of the CE stage and also increases the isolation between the input and the output of the cascode (increased stability). This is achieved without sacrificing mid-band gain since the collector of the CB stage carries a current almost equal to the collector current of the CE stage. The CB stage acts essentially as a current buffer or impedance transformer, faithfully passing on signal current to a higher resistance load while presenting a low load resistance to the CE stage. The improved isolation results in the cascode being easier to match and more stable than a CE stage alone.

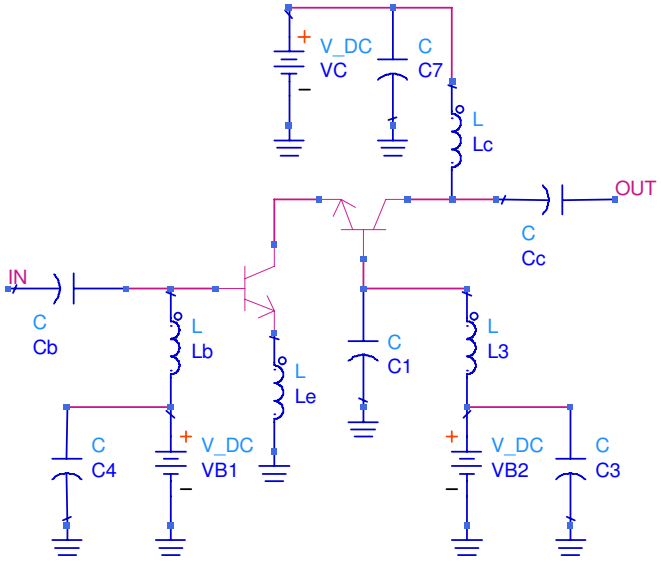


Figure 4: Cascode LNA topology

3.1.3 LNA Topology

The topology of the cascode LNA is shown in Figure 4. Traditionally, in addition to inductor L_b, there is another matching inductor in series with capacitor C_b. These input inductors have been combined to a single inductor (L_b) to reduce the input series resistance and thus achieve a lower noise figure (NF). Since the input and the output are well isolated (due to reduced Miller effect) each element can be used to tune a performance parameter independently:

CE transistor is sized for R_{opt} and thus minimum NF

CB transistor is sized for a low resistance presented to output of Q_1

The value of L_e determines R_{in}

The values of L_b and C_b determines X_{in}

The value of L_c determines R_{out}

The value of C_c determines X_{out}

The remaining elements do not have much effect on the performance parameters.

3.1.4 Realizable Range of the Lumped Elements

Not all values of lumped elements may be realized in the SiGe process, therefore, it is important from the outset to determine the realizable range for these elements. A variety of factors contribute to these ranges, but for this design the available capacitors and inductors (at 5 GHz) are limited to 0.104-2.732 pF and 0.3-4.438 nH, respectively.

In both cases, a minimum self-resonant frequency of 18 GHz was selected so that the inductance or capacitance remains relatively constant with frequency around 5 GHz.

3.1.5 Interconnects

The lumped elements and transistors were interconnected using 50 Ω thin film microstrip (TFMS) line. The design uses TFMS with the signal line on the top metal layer and the ground on the bottom metal layer. The maximum ground plane width is limited to avoid the need for stress relief slits. The ground plane is solely used under the interconnecting TFMS lines; there is no ground plane under the lumped elements nor within 10 µm of any lumped element because the lumped element models from the foundry do not include a ground plane.

The TFMS interconnects are simulated using the MLIN element in Agilent ADS. Momentum electromagnetic simulations were not performed. Parasitic extraction was also not performed. The allowable DC current on a 50 Ω TFMS line at 85ºC is sufficiently higher than the current in the LNA.

3.1.6 Transistor and Bias Selection

NPN transistors were selected for this design. They were modeled in ADS using a Hicum model provided by the foundry with the model substrate node connected to a 0V DC source based on a foundry recommendation. A single finger transistor with an emitter width of 0.3 µm (for lowest noise) and an emitter length of 1.9 µm was selected as the reference size.

The LNA biasing was determined by first selecting V_{CE}=1.5V for class A operation and also V_C=3V (2 “AA” batteries) for the cascode. Then V_{BE}=0.86V was chosen for the lowest minimum noise figure (NF_{min}) using the simulations shown in Figure 5 of NF_{min} v. V_{BE} at 5 GHz for the reference-sized NPN in common emitter configuration and using perfect choke/bypass/blocking elements.

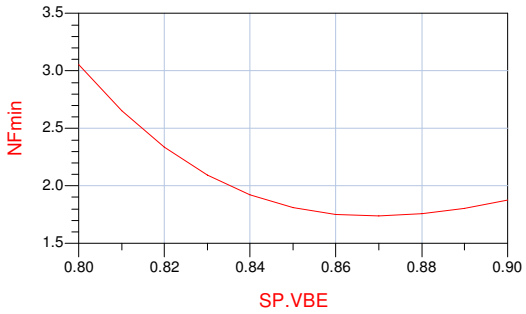


Figure 5: Simulated minimum noise figure v. bias

For simplicity, and low noise, the same bias point (V_{BE}, V_{CE}) was chosen for both the common emitter (CE) and common base (CB) stages. Hence, V_C=3V, V_{B1}=0.86V, V_{B2}=2.36V for the cascode configuration of the CE and CB stages.

3.1.7 Cascode Device Sizing

Using the chosen bias, a cascode of reference NPNs with no matching, ideal dc blocking and ideal choke elements, was simulated. The result was a simulated NF_{min} = 1.592 dB which occurs for a simulated Z_{opt} = 39-j341 Ω. The transistor size was then scaled for an optimum noise input resistance of R_{opt} 50 Ω for simultaneous input and noise matching. This scaled size is a 20.3 µm emitter length with the 5 base fingers.

The simulated performance of a cascode of scaled NPNs, with no matching and ideal blocking/choke elements, is NF_{min} = 1.683 dB with Z_{opt} = 60+j36 Ω. The real part of Z_{opt} is higher than 50 Ω and allows for the added resistance of interconnects and input matching lumped elements that lower the input resistance of the LNA.

The simulated maximum available gain (MAG) is 29.8 dB for the scaled cascode pair. Finally, the scaled cascode pair is unconditionally stable with stability parameters K>1 and B_1>0 (simulated K=2.042 and B_1 = 0.163) since the CB stage is presenting a low impedance to the CE stage.

3.1.8 Cascode Interconnects and CB Stage Base Bypass and Choke

Before the input and output matching circuits were designed, interconnecting TFMS lines were added to the design between all elements. The length of these lines, 100 µm, was fixed to provide spacing between the elements. Due to this short length (which is electrically short at 5 GHz), their impact on the performance was minimal.

The bypass capacitor (C_1) and the choke inductor (L_3) connected to the base of the CB stage were both selected prior to the input/output matching, with the maximum realizable values being used for both (2.732 pF and 4.438 nH, respectively). Using a higher capacitance doesn't really affect the cascode resistance and a lower bypass capacitance increases the output resistance of the cascode pair and means that a lower output inductor (L_c) can be used for the output match to 50 Ω. This lower output inductor will have a lower series resistance associated with it which increases the MAG of the overall LNA. Finally, the series resistance of the choke inductor was about 16.8 Ω, however this does not affect the cascode performance.

3.1.9 Cascode Output Matching

The output matching is achieved using L_c and C_c. Initially, ideal inductor and capacitor elements in ADS were used to tune the output match to 50 Ω. A 9 Ω series resistance was assumed for L_c based on simulations of the foundry inductor models. Changing L_c tuned the real part of Z_{out} whereas changing C_c tuned the imaginary part of Z_{out}. Once the values of L_c and C_c were determined for a 50 Ω output match, the equivalent foundry inductor and capacitor models that realize these values were used in the cascode design, resulting in a simulated cascode output impedance of 53-j3 Ω with an S_{22} of -27.3 dB.

3.1.10 Cascode Input Matching

The input matching is achieved using L_e, L_b and C_b. As with the output matching, ideal inductor and capacitor elements in ADS were used to optimize the input match to 50 Ω. Series resistances of 5 Ω and 1 Ω were assumed for L_b and L_e, respectively. Changing L_e tunes the real part of Z_{in}, whereas changing L_b and C_b tunes the imaginary part of Z_{in}. At this stage the optimizer was used for the first time in the design process, and once the values of L_e, L_b and C_{blk} were determined for a 50 Ω input match, the equivalent foundry inductor and capacitor models that realize these values were used in the design. This resulted in a simulated cascode input impedance of 58-0j Ω and an S_{11} of -22.4 dB.

3.1.11 Simulation of the Full Cascode LNA with Foundry Models

The full cascode LNA was simulated in Agilent ADS with foundry models for the lumped elements and transistors. These results are shown in Figure 6 to Figure 9. Statistical simulations were performed using the foundry corner models which define the "corners" of the foundry process. These results are shown in Figure 10 to Figure 14 and show the possible variation (indicated by the arrow) of the performance from chip to chip.

Figure 6: Simulated noise figure

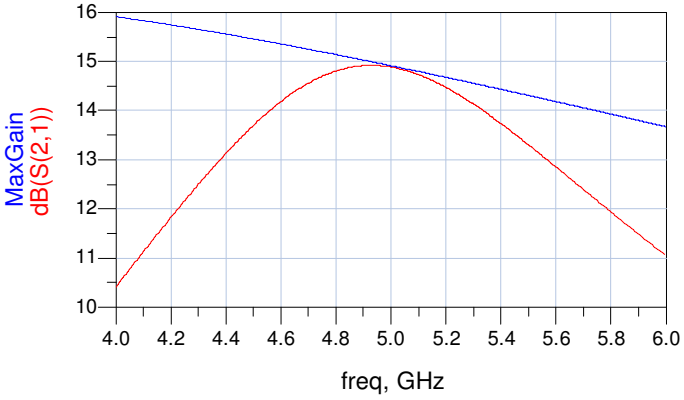


Figure 7: Simulated gain

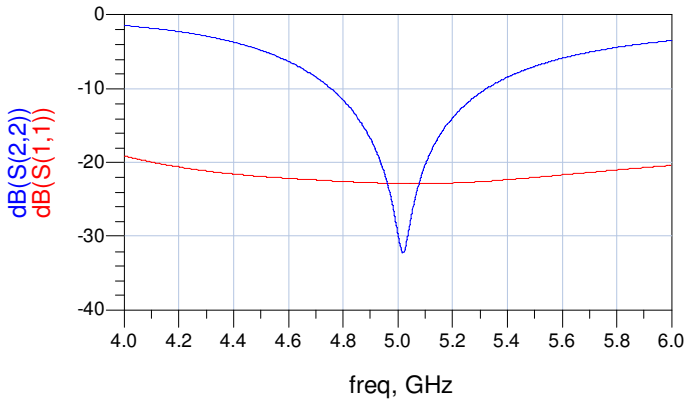


Figure 8: Simulated input and output match

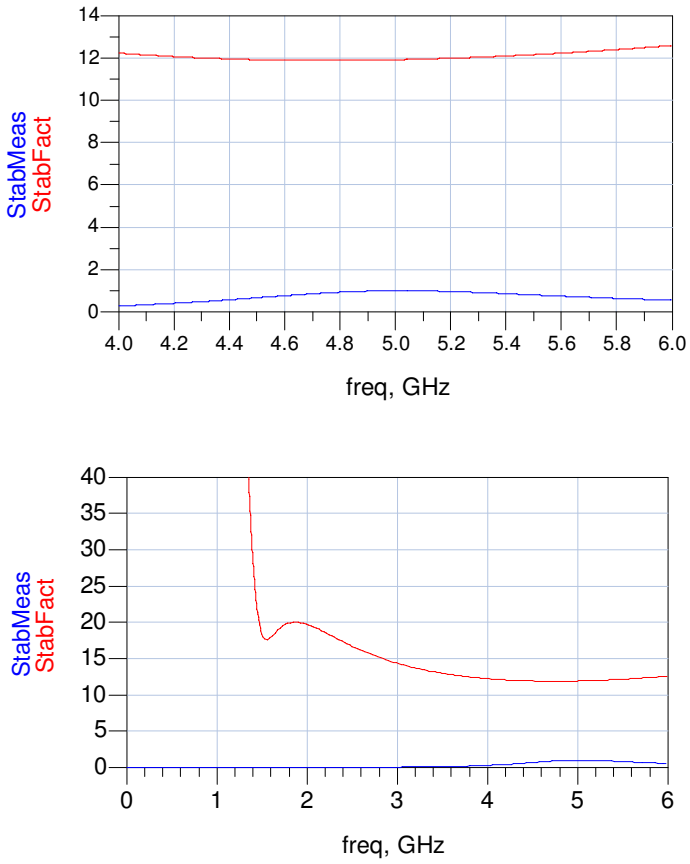


Figure 9: Simulated stability in-band (top) and at low frequency (bottom)

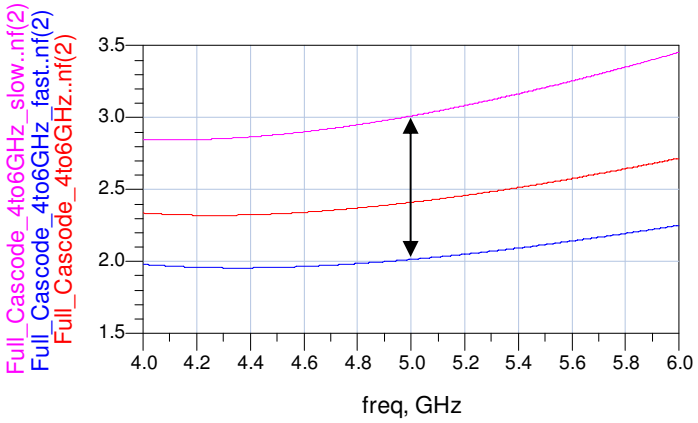


Figure 10: Statistical simulation of the noise figure

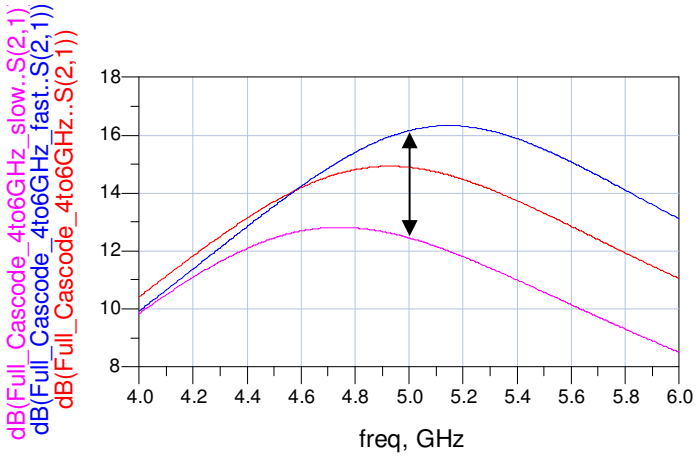


Figure 11: Statistical simulation of the gain

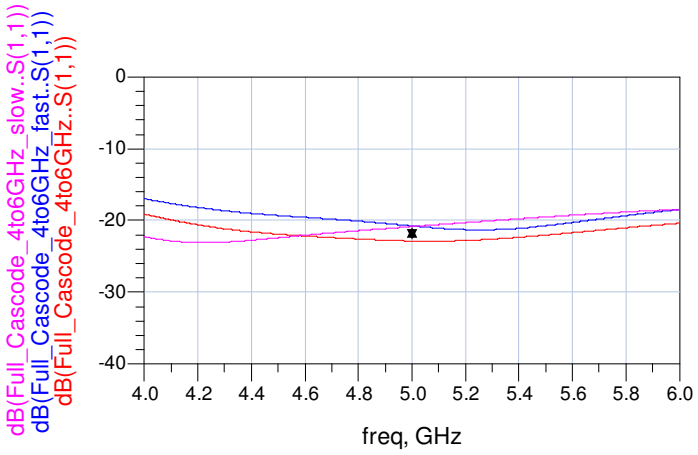


Figure 12: Statistical simulation of the input match

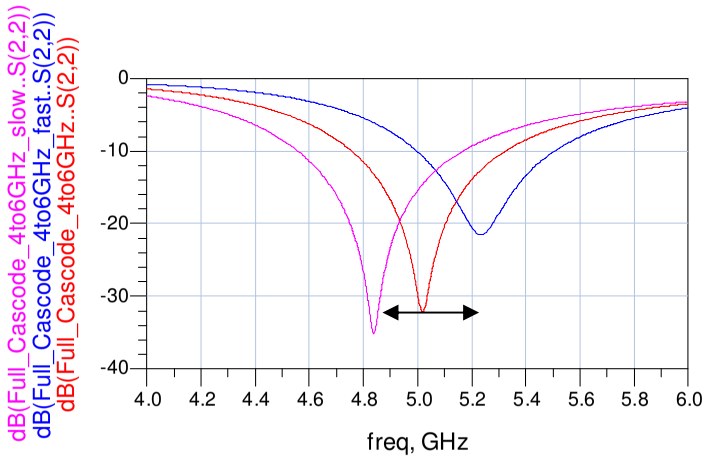


Figure 13: Statistical simulation of the output match

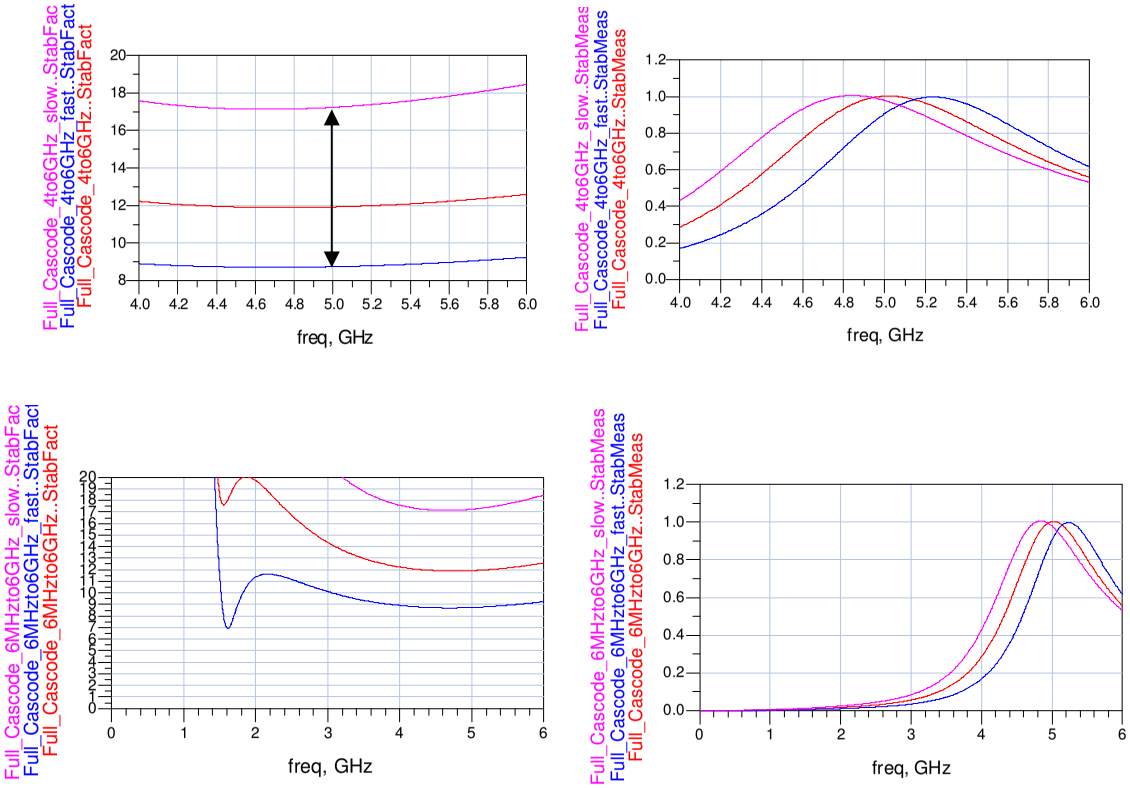


Figure 14: Statistical simulation of the stability

3.1.12 Fabrication of the LNA

Two versions of the LNA were fabricated by the foundry: one with and one without inductor guard rings. Photographs of these are shown in Figure 15.

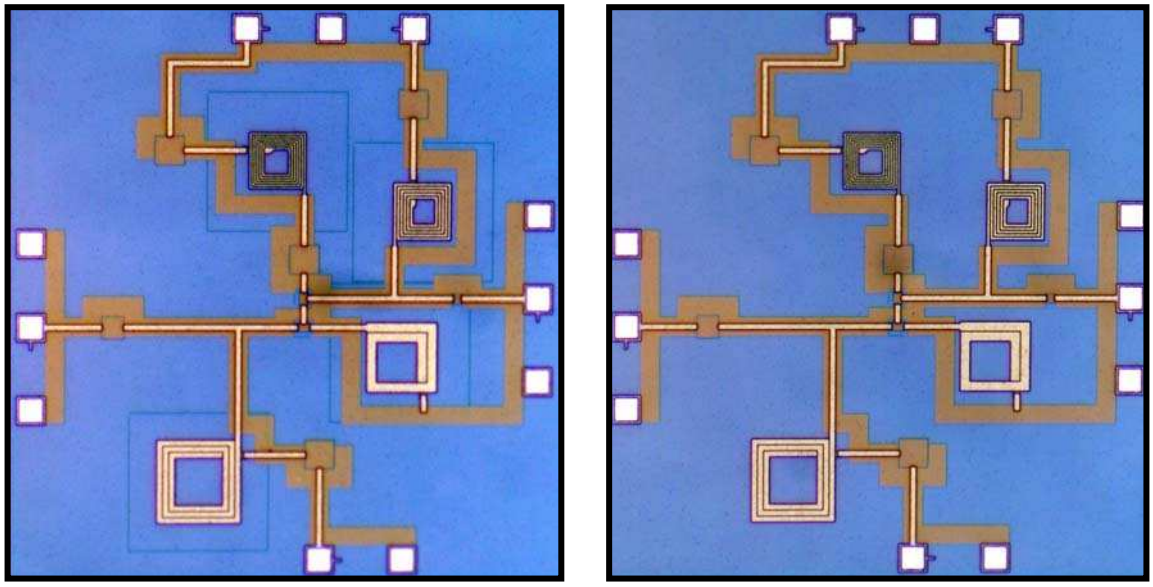


Figure 15: Photographs of fabricated LNA with (left) and without (right) inductor guard rings

3.1.13 Corrected Simulation Models

In February 2007, well after the LNA had been fabricated, the foundry released a design kit patch for ADS to improve the accuracy of the inductor models. The original models, used to design the LNA, were not as accurate as the models included in the Cadence design kit. Since the design of the LNA used less-than-accurate models, the performance of the LNA is expected to be worse than originally predicted in the previous sections. The actual performance of the inductors will be different from that originally predicted in the simulations hence the transistor will no longer be presented with the optimum impedance for minimum noise figure and maximum gain. Similarly, the return loss will also suffer.

3.1.14 VNA Measurements Compared to Original Foundry Models

The measured input match, output match and gain for both variations of the cascode LNA are given in Figure 16, Figure 17 and Figure 18. Five LNAs were measured using an Agilent 8510XF Vector Network Analyzer (VNA) with open-short-load-thru (OSLT) on-wafer calibration to the probe tips.

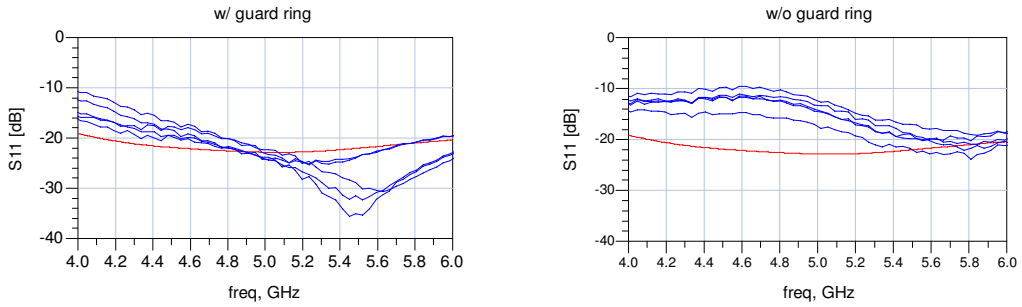


Figure 16: Input match – measurements (blue) and simulation with original models (red)

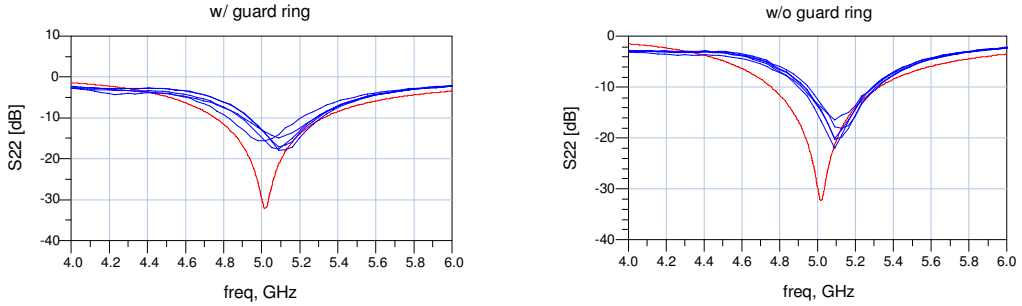


Figure 17: Output match – measurements (blue) and simulation with original models (red)

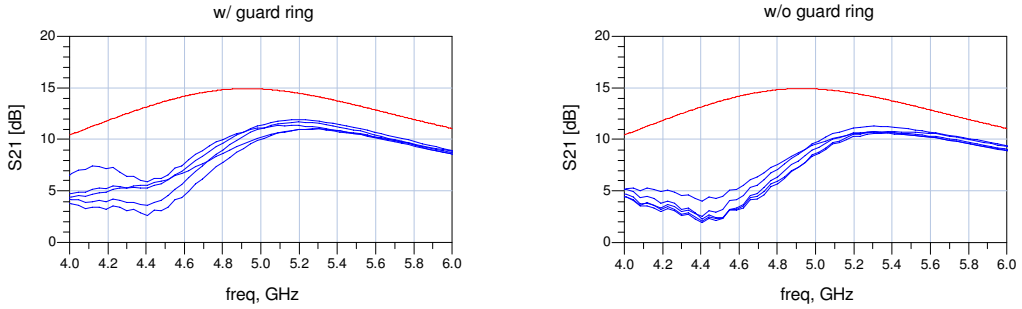


Figure 18: Gain – measurements (blue) and simulation with original models (red)

3.1.15 VNA Measurements Compared to Corrected Foundry Models

The LNA was re-simulated using the corrected foundry models and then compared to the measured performance (with guard rings). This comparison is shown in Figure 19, Figure 20 and Figure 21.

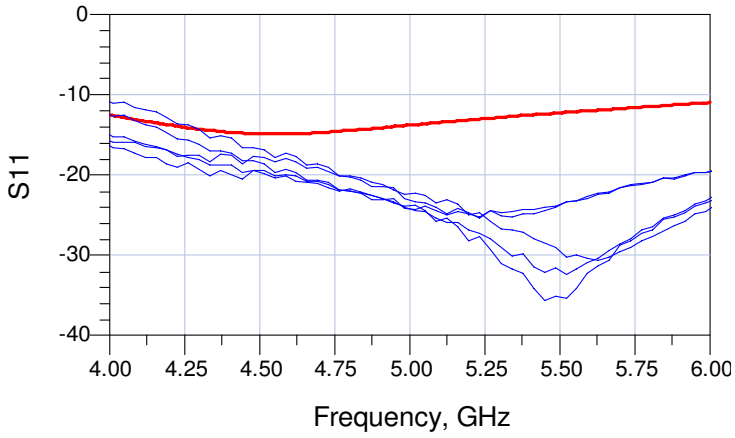


Figure 19: Input match (dB) – measurements (blue) and simulation with corrected models (red)

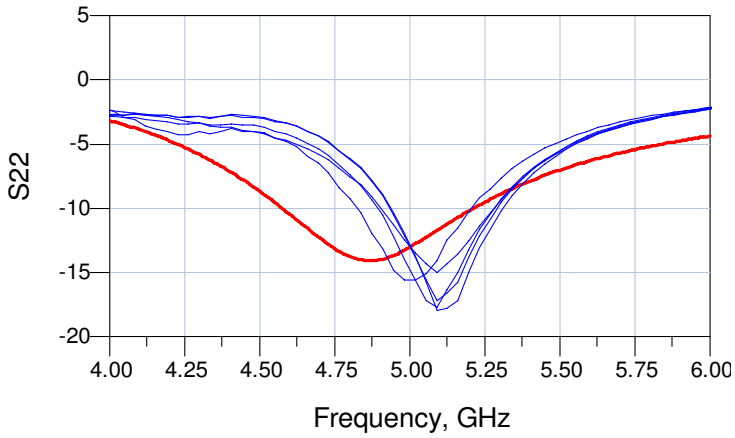


Figure 20: Output match (dB) – measurements (blue) and simulation with corrected models (red)

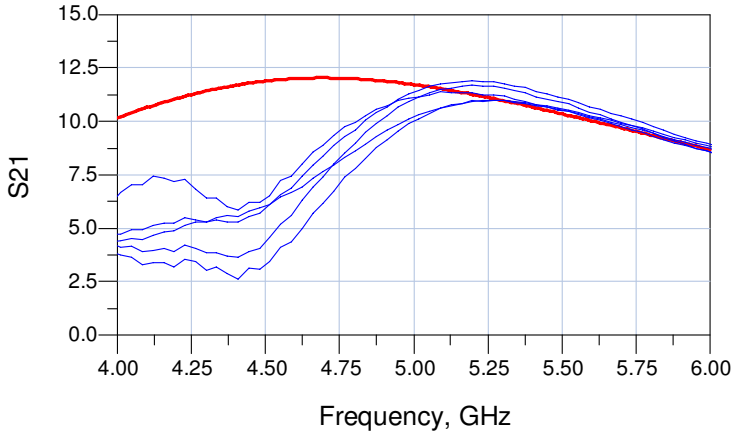


Figure 21: Gain (dB) – measurements (blue) and simulation with corrected models (red)

3.1.16 MXA Signal Analyzer Noise Figure Measurements

An Agilent N9020A MXA Signal Analyzer was used to measure the noise figure of three identical LNAs with guard rings. These results, shown in Figure 22, are also compared to simulations using the corrected models from the foundry. The simulated statistical variation using corrected foundry corner models is also shown. The MXA screen for one of the measurements (LNA #1) is shown in Figure 23.

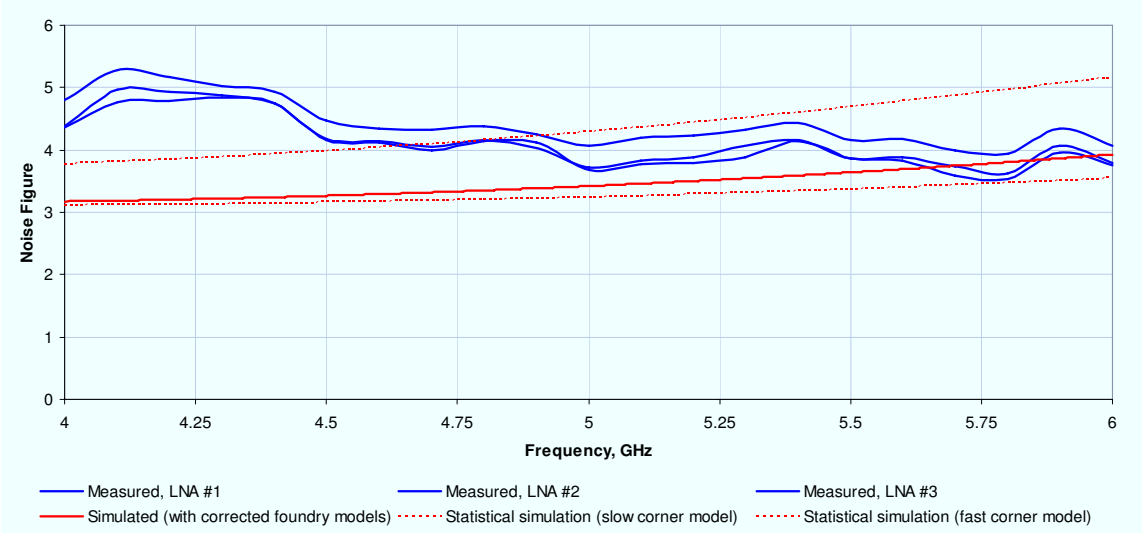


Figure 22: LNA noise figure – measured (blue) and simulated (red)

Figure 23: Agilent N9020A MXA Signal Analyzer screen shot for the noise figure measurement of LNA #1

3.2 Distributed Cascode LNAs at 20 GHz

3.2.1 Motivation

Millimetrewave integrated circuits are traditionally implemented using compound semiconductors such as gallium arsenide or indium phosphide. Silicon-germanium (SiGe) technology may well begin to intrude into this territory since both the transition and maximum oscillation frequencies of the most advanced SiGe bipolar transistors now exceed 200 GHz. Accordingly, there is a strong interest to use silicon technologies for integrated circuits at millimetrewave frequencies.

Recently, there has been renewed effort to implement traditional microwave passive circuits in monolithic silicon technologies. This can be challenging since on-chip passive device characteristics suffer from coupling to the silicon substrate. For example, due to the relatively high conductivity of the substrate in most SiGe processes, the lumped inductors have substrate-induced losses. The large capacitive coupling to substrate lowers the quality factor of these inductors, making inductor-based impedance matching networks difficult at millimetrewave frequencies. In light of this, a 20 GHz LNA using distributed passive elements was designed in a standard SiGe process in order to minimize the effects of the lossy silicon substrate.

3.2.2 Transmission Line Candidates

The choice of distributed transmission structures is illustrated in Figure 24. Their performance depends on number of metal layers, the metal conductivity/thickness, and the dielectric properties/thickness. Of the candidates shown in Figure 24, thin-film microstrip (TFMS, furthest left) is chosen here.

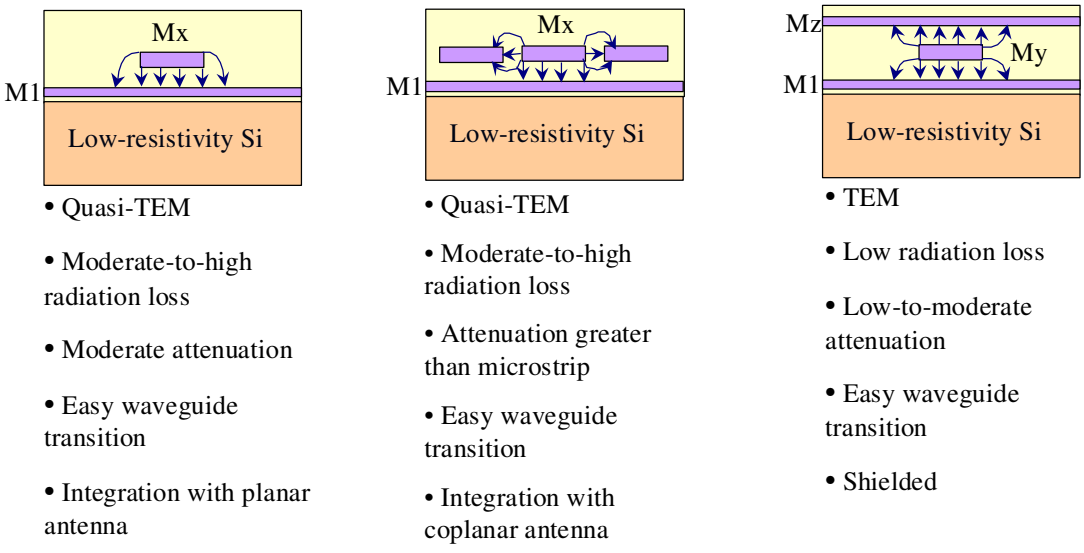


Figure 24: Potential transmission lines for silicon-based RFICs: microstrip (left), coplanar waveguide (centre) and stripline (right)

TFMS lines on silicon are typically implemented using the top-layer metal as the signal line, and the bottom-layer metal for the ground plane. In this configuration, shown in Figure 25, the bottom-layer metal acts as a shield with essentially no electric field penetration into the substrate. Furthermore, the silicon-based TFMS offers the following features:

1. TFMS can be meandered with spacing between adjacent lines of only 2 or 3 times that of the film thickness, which effectively miniaturizes transmission lines,

2. High-isolation TFMS crossovers can be made using narrow-width lines on two different layers, which adds layout flexibility, maintains high frequency operation, and achieves chip size reduction,

3. TFMS is "self" shielding (due to its ground plane) for low electrical loss, and

4. Low characteristic impedances are possible.

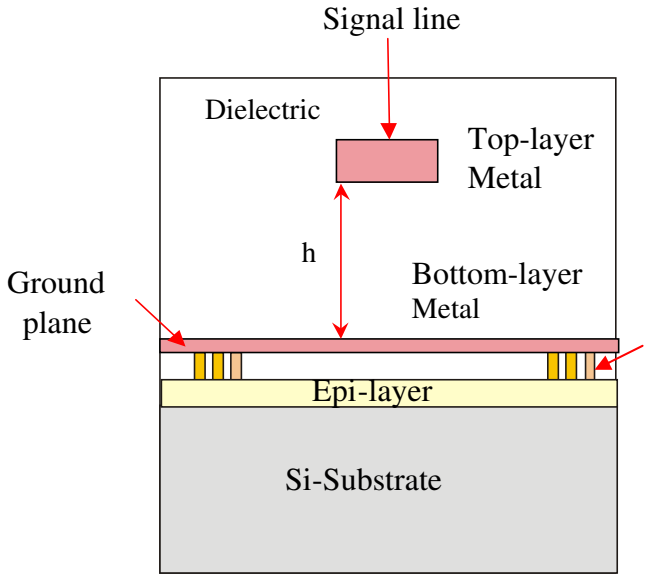


Figure 25: RFIC thin-film microstrip using a top-side ground

3.2.3 Single Stage 20 GHz SiGe Distributed Cascode Amplifier

The LNA is usually the first stage of any receiver. This stage provides enough gain to overcome noise of subsequent stages. It should offer as little noise as possible to large signals and at the same time provide good linearity. A narrowband cascode design topology was used here because of its good frequency performance. An LNA design presents a considerable challenge because of its simultaneous requirement for high gain, low noise figure, good input and output matching and unconditional stability at the lowest possible current draw. Although gain, noise figure, stability, linearity and input and output match are all equally important, they are interdependent and do not always work in each other's favour.

3.2.3.1 Design Requirements

The LNA specifications were:

Frequency range: 19~20 GHz

Input impedance Z_{in}: $|Z_{in}| = 50\ \Omega$

Output impedance Z_{out}: $|Z_{out}| = 50\ \Omega$

Voltage gain: $A_V > 10$ dB

Noise Figure: NF with 50 Ω input matching < 6 dB

3.2.3.2 Design Procedure

3.2.3.2.1 Circuit Topology Selection

It is well known that a common emitter stage, with its high input resistance and relative high voltage gain, is best suited for obtaining the bulk of the gain required for an amplifier.

A common base stage has an open circuit voltage gain almost equal to that of the common-emitter circuits. Its input resistance, however, is much smaller and its output resistance much larger than the corresponding values for the common emitter stages. These two properties make a common base stage suitable for a current buffer. Furthermore, the absence of the Miller effect in a common base circuit makes its high frequency response far superior to that of the common emitter amplifiers.

Thus, combining these two kinds of circuits together gives a cascode amplifier which gains the advantages of both the common emitter circuit and the common base circuit. The cascode configuration provides the high input resistance and large transconductance achieved by the common emitter stage with the superior high frequency response of the common base stage. In this LNA design, the cascode structure in Figure 26 is chosen as the topology of the LNA core circuit. Note that degeneration is avoided since the associated parasitics might destabilize the amplifier.

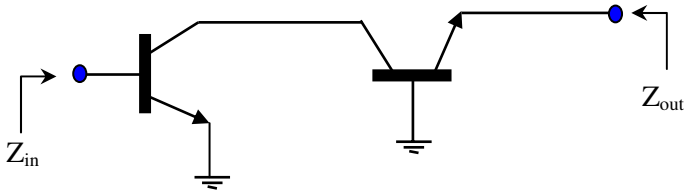


Figure 26: Core LNA circuit topology

3.2.3.2.2 HBT Cascode Characterization

The cascode configuration was characterized by simulating input and output impedance, as well as f_T and f_{max}. Figure 27 to Figure 29 show these parameters for the chosen transistor size, which is shown in Figure 27. This transistor size provides easy matching with reasonable gain at 20GHz.

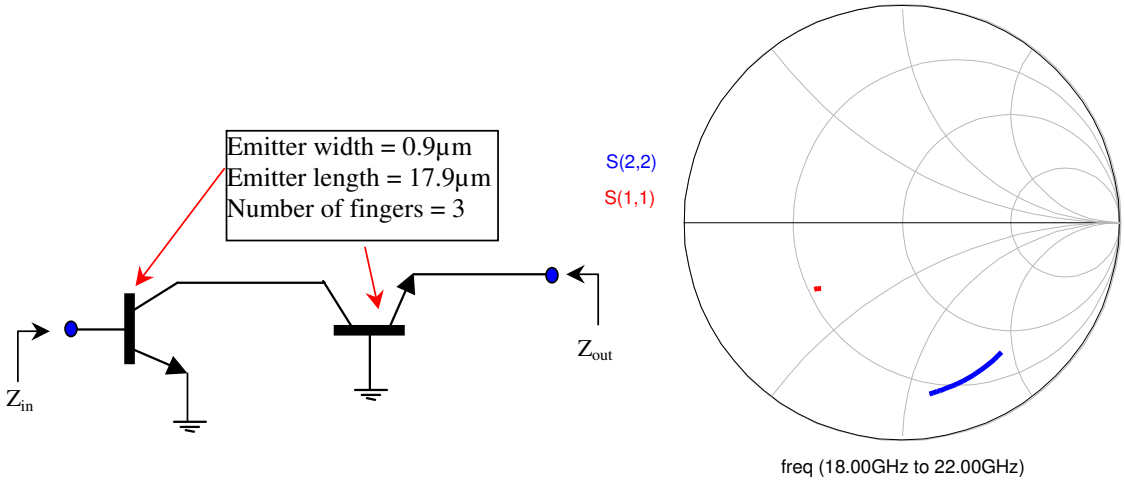


Figure 27: Z_{in} (S_{11}) and Z_{out} (S_{22}) versus frequency

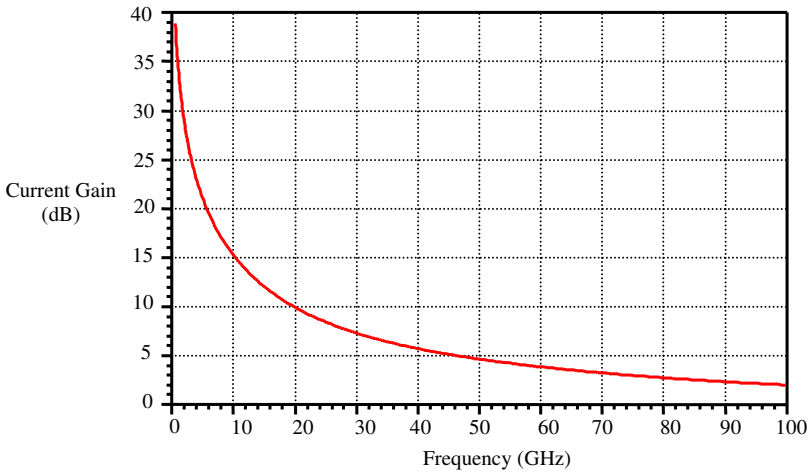


Figure 28: Cascode transistor characterization - simulated f_T

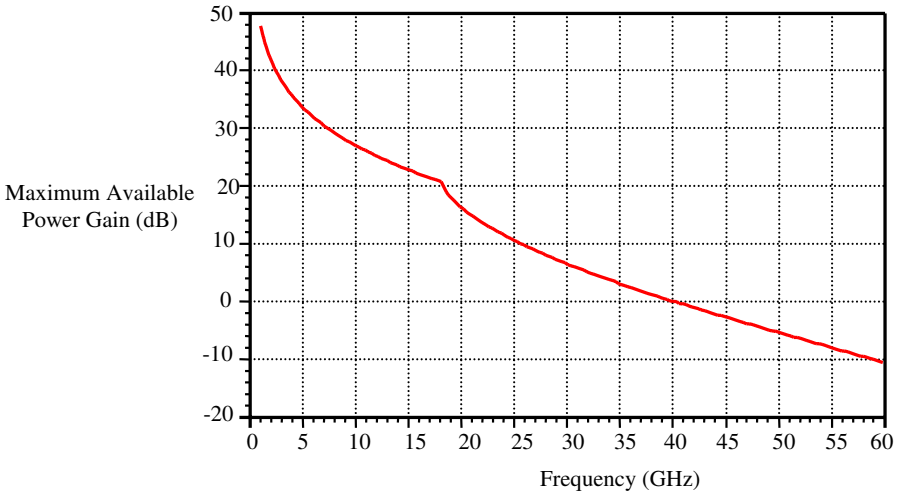


Figure 29: Cascode transistor characterization – simulated f_{max}

The complete distributed cascode amplifier is shown in Figure 30. The base bias voltage for the upper transistor was set to 2.45 V whereas for the bottom transistor the base voltage was 0.9 V. All matching components are realized by TFMS inductive and capacitive elements. TFMS is also used for interconnects and biasing.

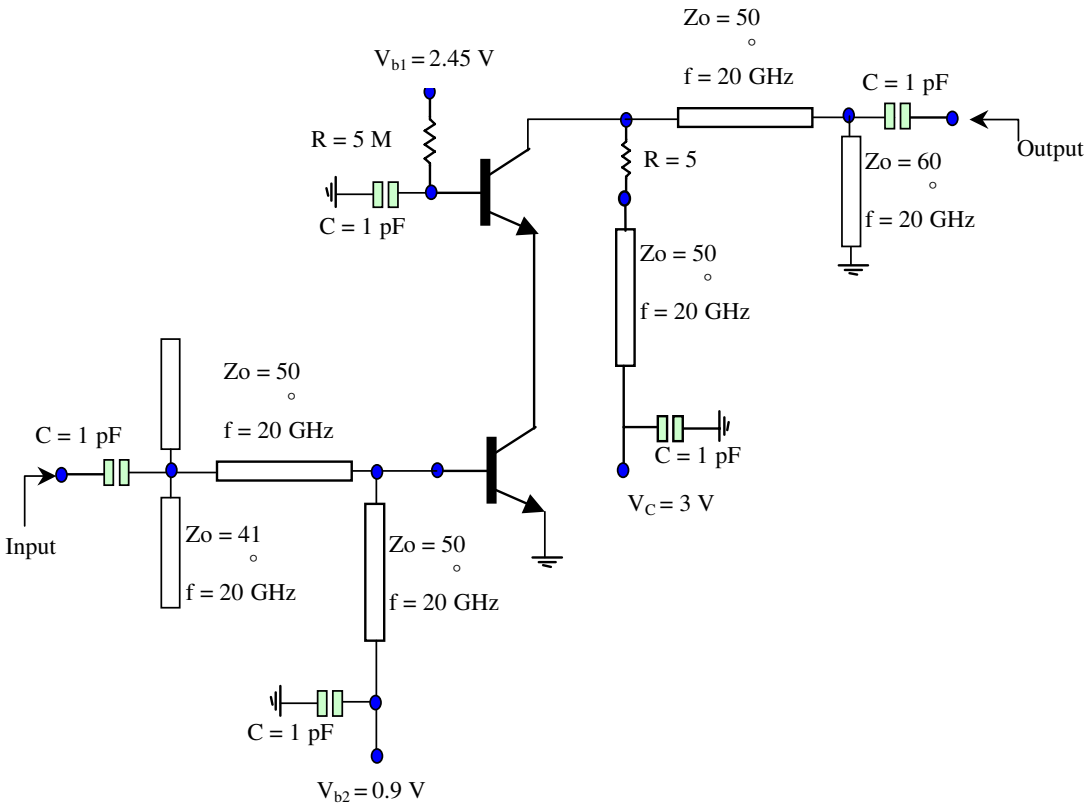


Figure 30: Distributed cascode amplifier schematic

3.2.3.3 Simulation Results

AC, noise and scattering-parameter (s-parameter) simulations were performed on the LNA using Agilent ADS. These analyses were done to determine the total current, voltage gain, input and output impedance and the noise figure of the LNA.

For the frequency range of interest, Figure 31 shows the voltage gain versus frequency, Figure 32 shows the simulated noise figure versus frequency and Figure 33 shows the return losses. At a frequency of 20 GHz the simulated results are: a gain of 10 dB, a low noise figure of 8 dB, an input return loss of 18 dB, and an output return loss of 12 dB.

Figure 34 shows that the distributed cascode amplifier is unconditionally stable.

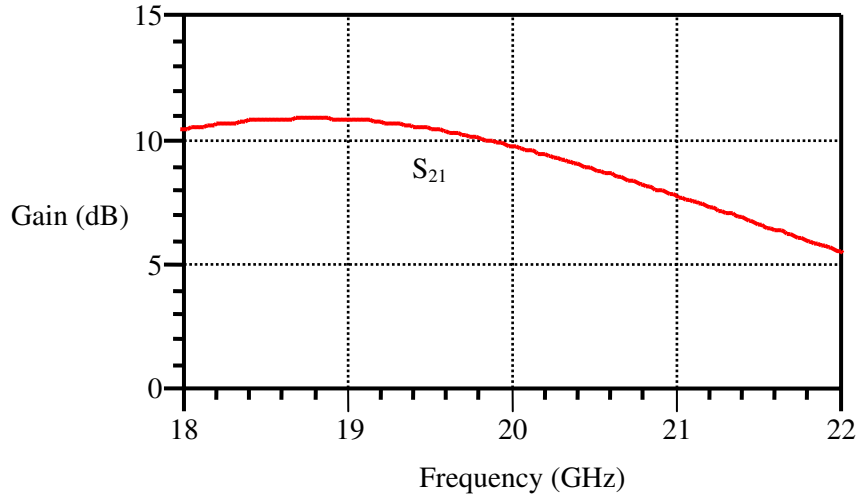


Figure 31: Simulated forward gain versus frequency

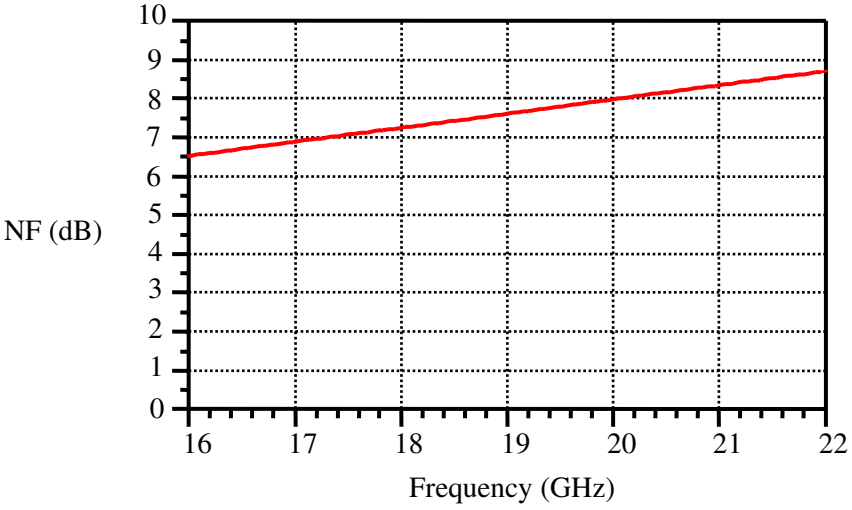


Figure 32: Simulated noise figure versus frequency

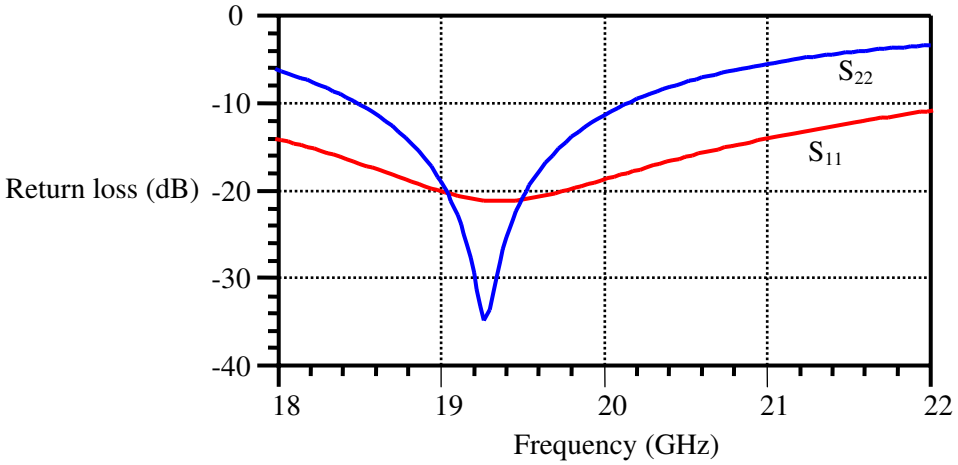


Figure 33: Simulated return losses

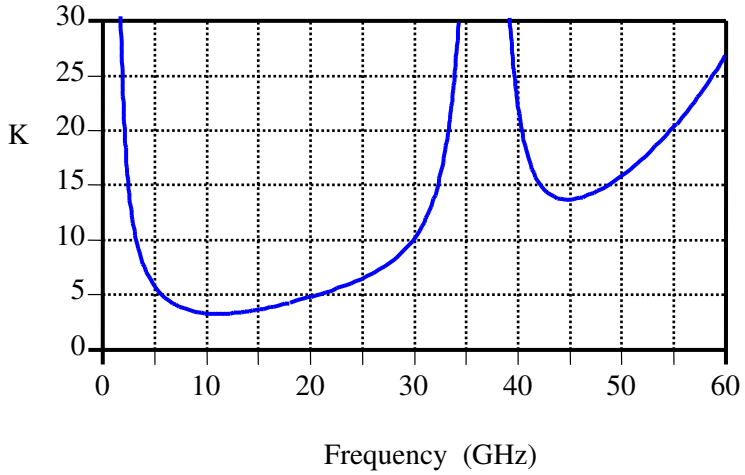


Figure 34: Simulated amplifier stability factor, K

3.2.4 Two Stage 20 GHz SiGe Distributed Cascode Amplifier

A two-stage cascode topology was designed to achieve higher gain and to minimize input mismatch over gain variations. The input matching is optimized to provide a compromise between the input reflection (S_{11}) and the noise figure (NF). For the selected transistors, the optimum noise figure matching point is very close to the conjugate-matching point, hence S_{11} and NF can be optimized simultaneously.

Note that even though a cascode topology reduces the feedback from the output of the LNA to the input, this feedback is still significant at 20GHz. Consequently, the choice of the load reflection coefficient does affect the source reflection coefficient required for input matching.

Meandered thin film microstrip transmission lines are used as matching components to decrease the LNA size. Capacitive coupling is used throughout to eliminate DC offsets between stages.

3.2.4.1 Simulation Results

The simulated forward gain of the two-stage distributed cascode amplifier is shown in Figure 35. The gain at 20 GHz is 18.2 dB and it varies by 1.3 dB from about 19 GHz to 20.5 GHz. The majority of the gain arises from the cascode second-stage. The peak gain occurs at 19.3 GHz.

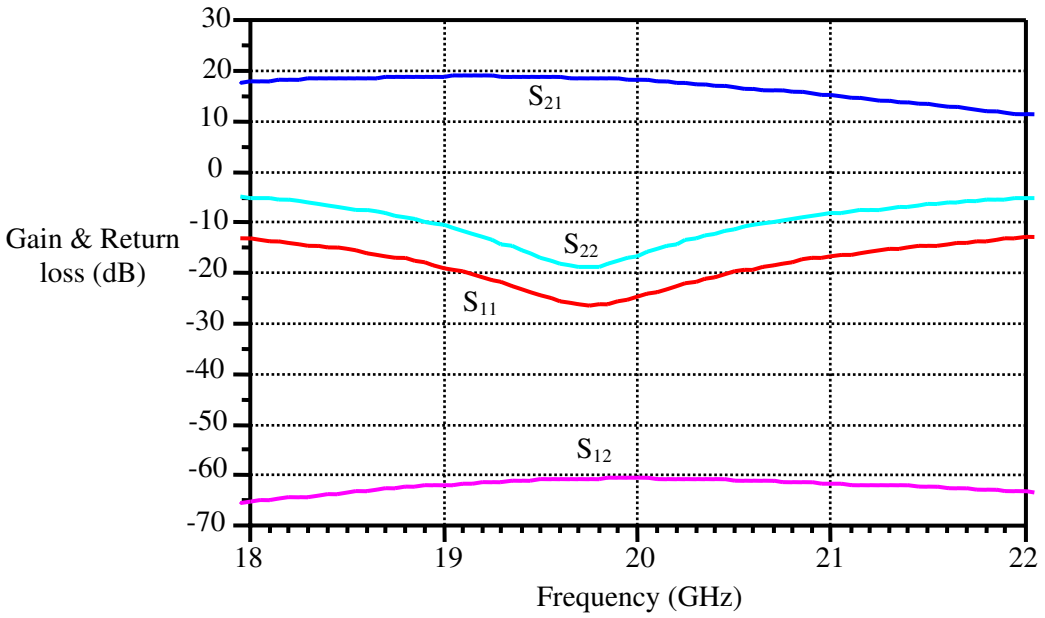


Figure 35: Simulated return losses, and forward/reverse gain, for the two-stage, distributed cascode amplifier

Figure 35 shows the simulated S-parameters S_{11}, S_{22} and S_{12} for the two-stage distributed cascode amplifier. Both S_{11} and S_{22} are well below -10 dB from about 19 GHz to 20.5 GHz, indicating good input and output power matches. The values for S_{11} and S_{22} at 20 GHz are -25 dB and -17 dB respectively. The reverse gain (S_{12}) is shown for completeness and is below -60 dB for the entire 1.5 GHz bandwidth. Both the cascode structure of the second-stage, and the fact that the LNA consists of two separate stages, are what make this very low level of reverse leakage possible.

Figure 36 plots the simulated NF and NF_{min} for the two-stage distributed cascode amplifier. The simulated noise figure at 20 GHz is 8.7 dB. The difference between the LNA noise figure and minimum noise figure curves at this frequency is only 0.3 dB. This indicates a very strong noise match for the two-stage distributed cascode amplifier.

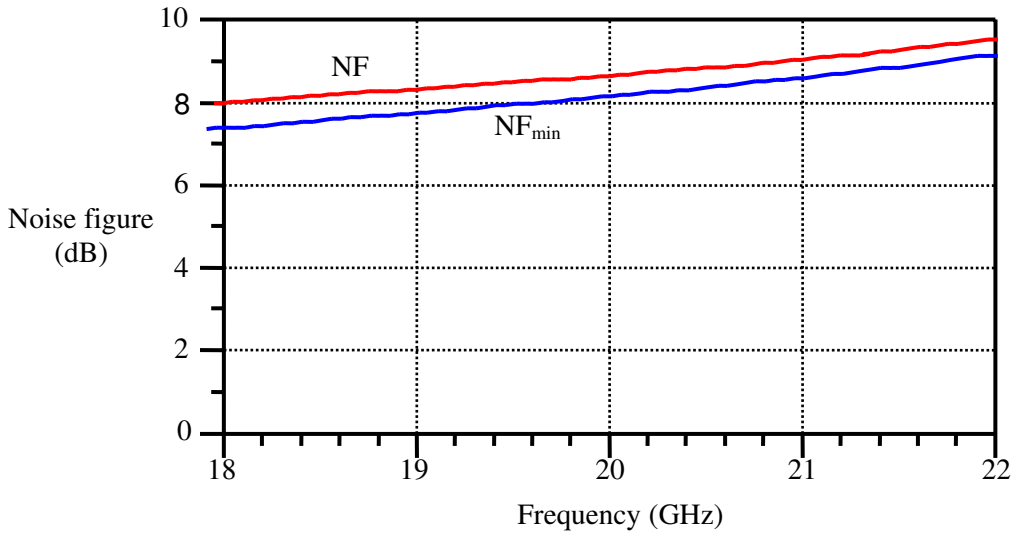


Figure 36: Simulated noise figure versus frequency for the two-stage distributed Cascode amplifier

3.2.5 Fabrication of One- and Two-Stage 20 GHz Distributed Cascode SiGe Amplifiers

Both one- and two-stage 20 GHz distributed cascode amplifiers were fabricated by the foundry, photographs of which are shown in Figure 37 and Figure 38, respectively. The single-stage LNA occupies an area of 0.56× 0.58 mm^2 and the two-stage LNA occupies an area of 0.66 × 0.72mm^2 (including pads).

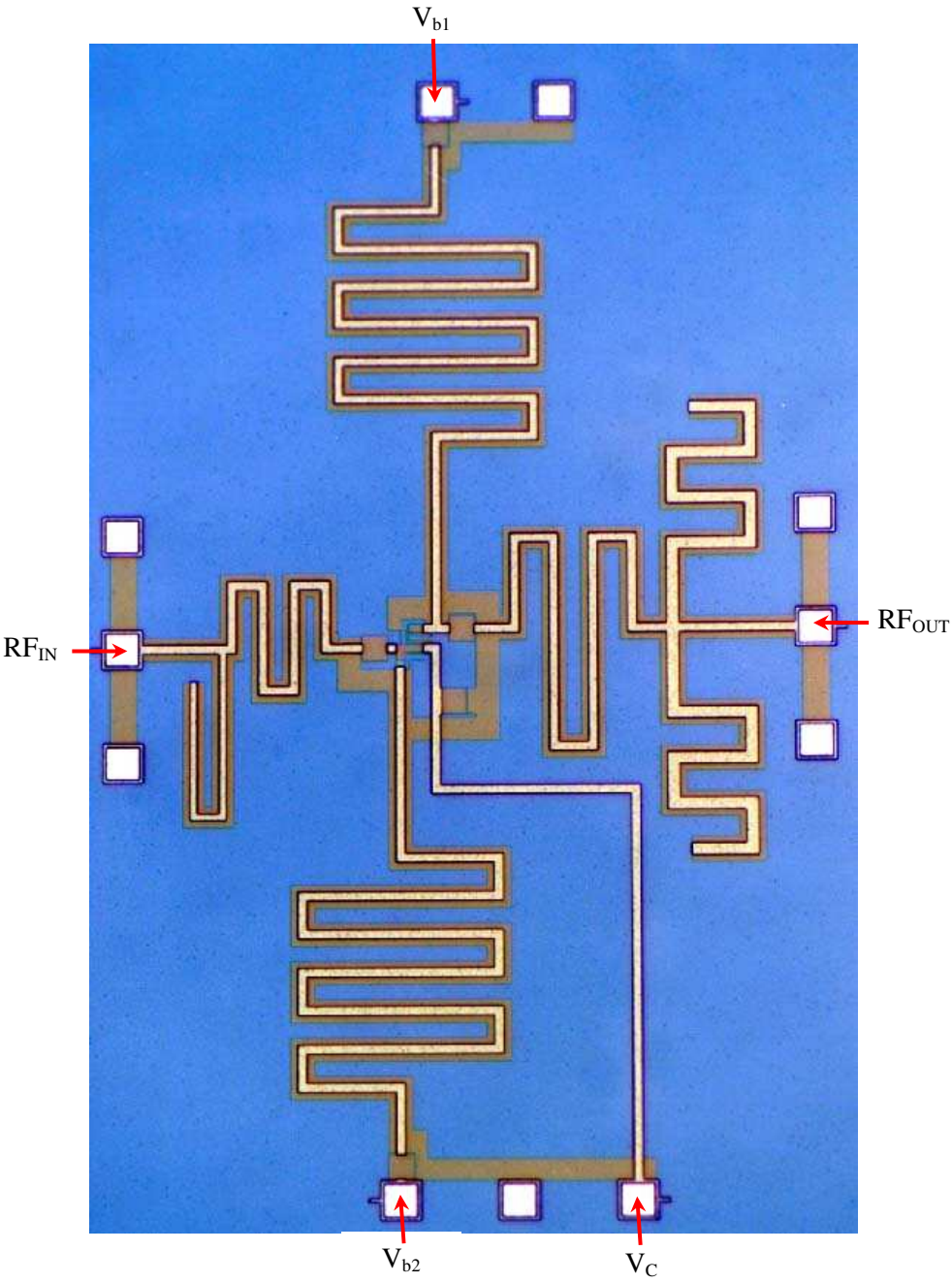


Figure 37: Die photo of a 20 GHz single-stage, distributed cascode amplifier

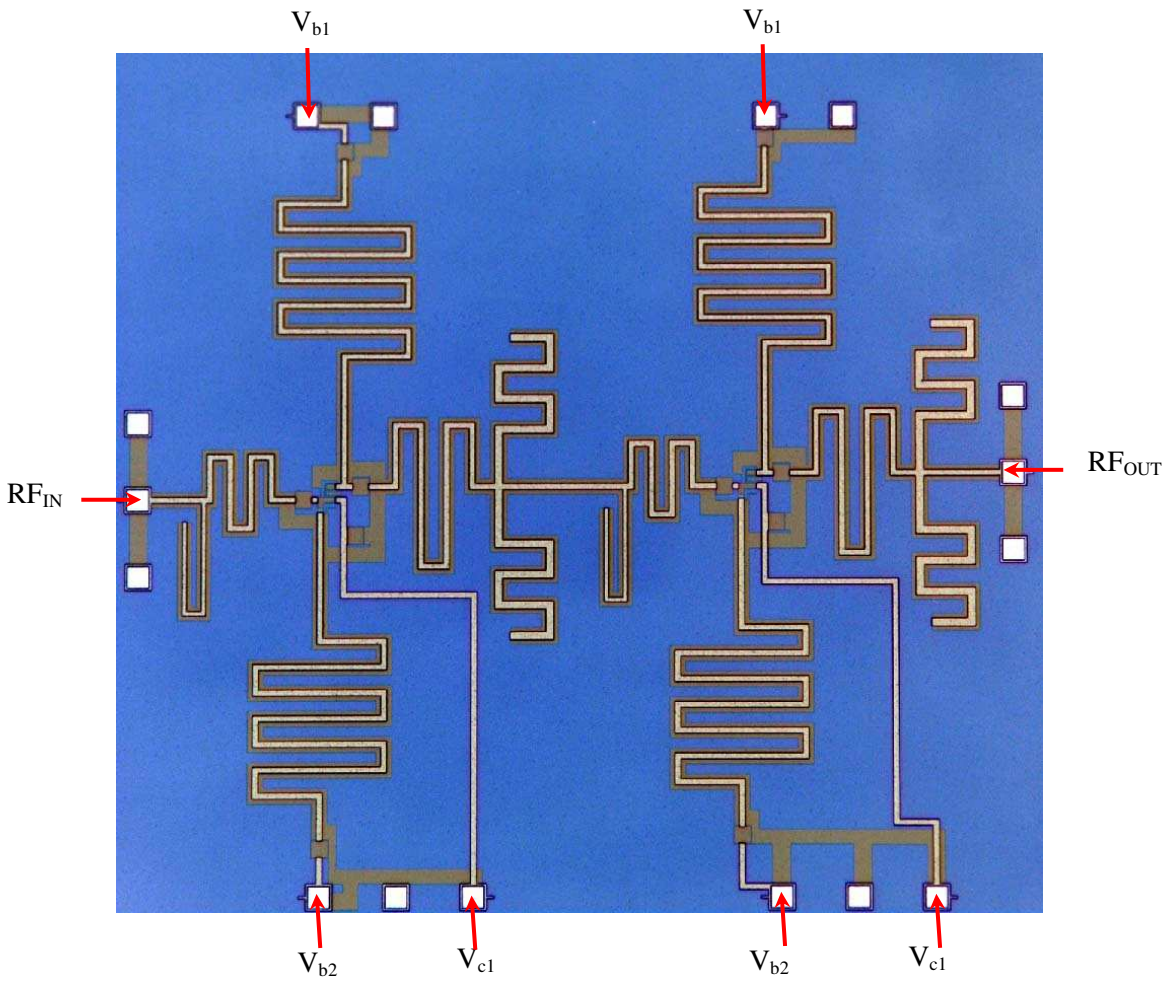


Figure 38: Die photo of a 20 GHz two-stage, distributed cascode amplifier

3.2.6 Experimental Results

Since layout versus schematic (LVS) was not possible for the 2005 tape-out, a short circuit in the layout of the cascode distributed amplifiers was not detected. As a result, the circuit in question was inoperable and could not be adequately tested or characterized. This short circuit fault was corrected and the single-stage distributed cascode LNA was included in the 2006 tape-out (which did include LVS) and could therefore be successfully tested. This characterization was performed on wafer with an HP8510 network analyzer, Cascade Microtech AirCoplanar GSG probes, and a DC probe card with 100pF bypass capacitors located at each of the four power pins. With the RF pads having been incorporated into the on-chip matching networks, no de-embedding was performed on the measured data. The measurement system was calibrated to the probe tips using an open-short-load-thru on-wafer calibration.

The measured forward and reverse gain of the 20 GHz single stage distributed cascode amplifier is shown in Figure 39. The measured gain of 0.5 dB at 19 GHz is about 10 dB lower than the gain

predicted by simulation. Inaccurate transistor models could account for the difference since the 0.35 µm SiGe HBT process isn't generally suitable for RFIC design applications above 10 GHz. Therefore, because for low measured gain, the noise figure was not measured.

The measured input match and output match for the distributed cascode amplifier is also given in Figure 39. The minimum return loss is 12 dB at 19 GHz for S_{11} and S_{22}.

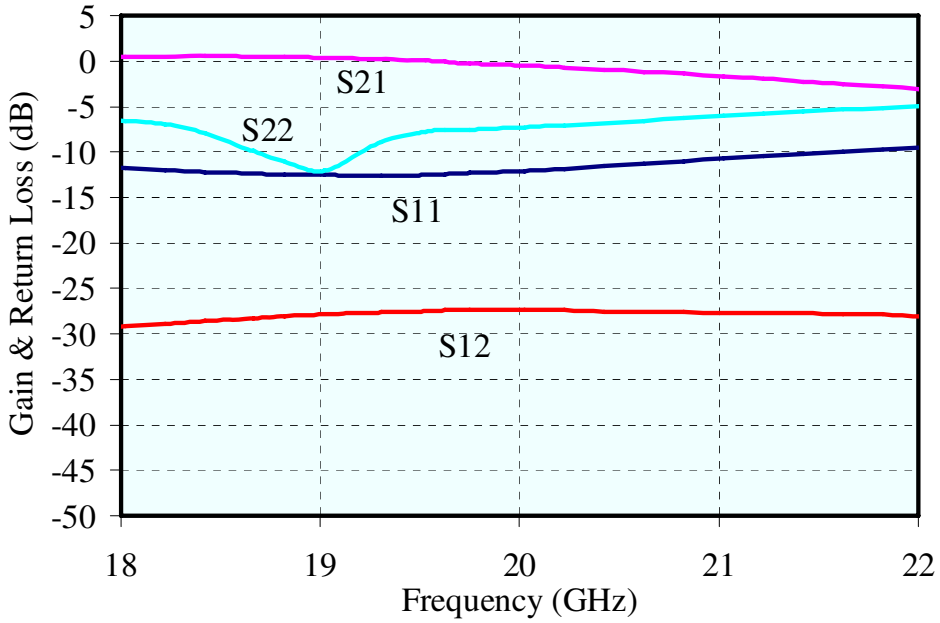


Figure 39: Measured return losses, and forward/reverse gain, for the single-stage, distributed cascode amplifier

4 Nonlinear RFICs

4.1 Differential VCO at 5 GHz with Buffer Amplifiers and Current Source Noise Filtering

4.1.1 Introduction

This section describes the design and measured performance of a 5.1 GHz differential LC voltage controlled oscillator (VCO) fabricated using a 0.35 µm silicon germanium (SiGe) heterojunction bipolar transistor (HBT) process. The VCO design was simulated in Agilent ADS, laid out in Mentor Graphics IC Station and verified using Mentor Graphics Calibre. The tape-out was Dec. 2006.

4.1.2 VCO Topology

The VCO topology, shown in Figure 40, is a differential LC oscillator having a cross-coupled differential pair and a resonant inductor-capacitor (LC) tank. At resonance the LC tank has a 0º phase shift whereas the cross-coupled pair has a 360º phase shift, thus the oscillatory condition is satisfied (assuming the cross-coupled pair has also saturated).

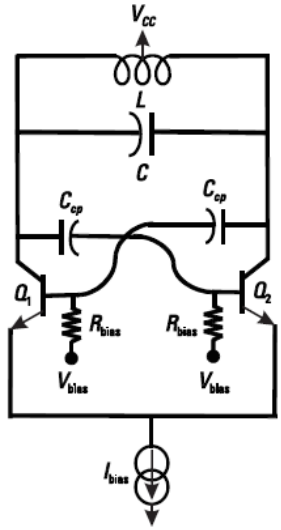


Figure 40: VCO topology

The base-collector of each transistor is decoupled using two capacitors (C_{cp}) to increase the output power of the oscillator. The capacitor in the LC tank is implemented using a varactor so the oscillation frequency can be tuned. A differential inductor is used in the LC tank allowing the collector bias voltage (V_{cc}) to be injected at the centre tap so that no RF choke is required. The base bias voltage (V_{bias}) can be fed through RF blocking resistors (R_{bias}) because the base current is small. A current source sets the tail bias current (I_{bias}). Two buffer amplifiers (not shown in

Figure 40) connected to each collector match the differential output to 50 Ω without loading the oscillator.

4.1.3 Cross-Coupled Differential Pair

The base-collector decoupling capacitors are 2.741 pF (the maximum realizable capacitance value at 5.1 GHz, see also Section 3.1.4). The large capacitance is required for a low impedance in the RF signal path. These capacitors allow the base and collector of the devices to be independently biased to increase the output power of the VCO.

Each HBT base is biased at 1V (slightly above the base-emitter diode drop) using 5 kΩ choke resistors. High value unsalicided poly resistors are used with $R_{5.1GHz}$=4905 Ω with the variation from 4-6 GHz being about 100 Ω. The resistors were short (w=2 µm, l=8 µm) because the foundry models are more accurate for shorter resistors.

The cross-coupled differential pair is a negative resistance cell for the oscillator and thus provides power to the LC tank. The negative resistance can be simulated as shown in Figure 41 where each device has 5 base fingers, a nominal bias current of 18 mA, and an emitter length (el) varying from 5.1 to 20.3 µm. Figure 41 shows that as device size increases, $|R_{neg}|$ decreases while the parasitic capacitance increases as shown in Figure 42. Note that this capacitance will limit the tuning range by lowering the impact of the varactor capacitance changes.

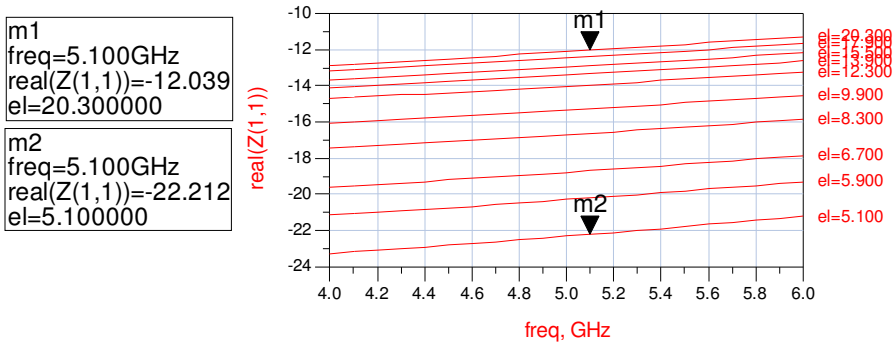


Figure 41: Simulated negative resistance of a cross-coupled differential pair

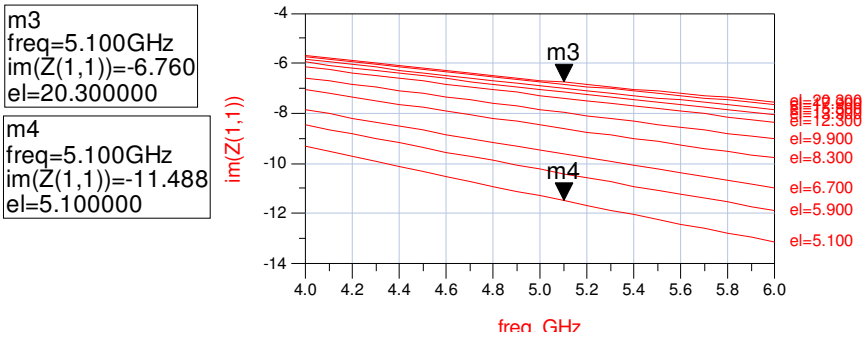


Figure 42: Simulated parasitic capacitance of a cross-coupled differential pair

4.1.4 Differential Tank Inductor

Ideally, it is desirable to simultaneously maximize the inductor quality factor Q (for low phase noise) and inductance L (for high output power); however, this isn't possible since the higher the inductance, the lower the Q. Since a lower inductance can be compensated by an increase in I_{tail} to maintain the same output amplitude (and the same phase noise), the Q of the inductor was maximized despite any drop in inductance since there is no requirement to limit I_{tail} for DC power consumption.

Therefore, a differential inductor from the over 4000 available in the 0.35 µm SiGe process was chosen for maximum Q_{peak} at F_{peak}=5.1 GHz with self-resonant frequency (SRF)>20 GHz. Specifically, a differential inductor was selected with outside dimensions (x and y)=175 µm, conductor width (w)=20 µm, conductor spacing (s)=2 µm, and number of turns (n)=2. Simulated results are Q_{peak}=12.6 at F_{peak}=5.1 GHz with SRF>27 GHz and $L_{5.1GHz}$=0.626 nH with $R_{S,\ 5.1GHz}$=1.591 Ω as shown in Figure 43 and Figure 44. Other combinations of parameters are possible; however, they do not increase Q_{peak} and they may occupy more circuit area. When used in an LC tank, and close to resonance, this differential inductor presents an approximate effective parallel resistance of $R_p \approx Q^2 R_s = 12.6^2 \times 1.591 = 252\ \Omega$.

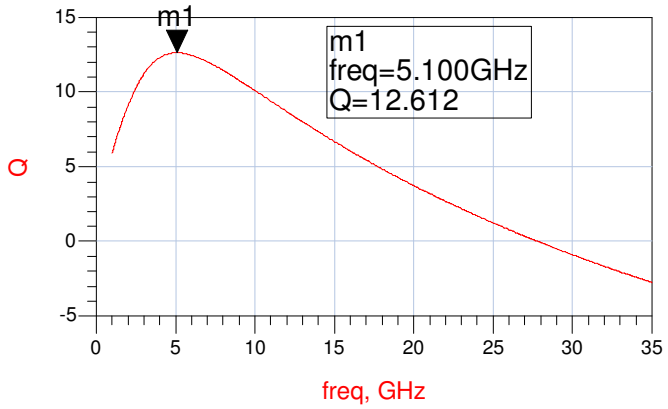


Figure 43: Simulated peak Q for the differential tank inductor

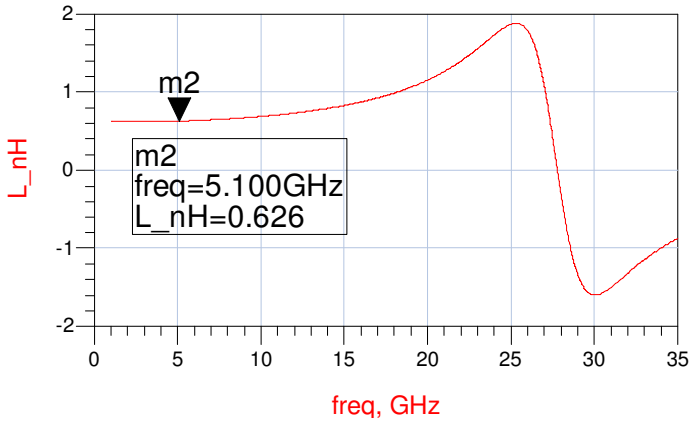


Figure 44: Simulated inductance for the differential tank inductor

4.1.5 Tank Varactor

A PN junction varactor was chosen to vary the tank capacitance and hence also the oscillation frequency. Three parameters, the finger width W_d, the finger length L_d and the number of fingers N_a, can be used to set the capacitance. Initially, W_d and L_d are chosen and N_a is used to re-adjust the capacitance at each step in the VCO design to ensure the correct oscillation frequency at the centre of the tuning range.

A typical value of W_d=1.5 μm was chosen which is close to the minimum size for maximum possible varactor Q. A L_d of 50 μm was also chosen and this is needed to achieve the required capacitance to resonate with the differential inductor. Finally an N_a of 25 was chosen, which can be adjusted between 2 and 50 to allow fine tuning of the tank capacitance during the later stages of the design.

With W_d=1.5 μm, L_d=50 μm and N_a=25, the small-signal varactor Q varies from 21-43 over a tuning range 0-2.5 V. This corresponds to a small-signal capacitance that varies from 2.1-4.4 pF. The worst case small-signal Q of 21 still almost twice the inductor Q of 12.6, so the oscillator tank Q is still dominated by the inductor with only a slight reduction to 8.4 (where 21||12.6 = 8.4).

The small-signal capacitance over the tuning range is not linear and not symmetric about 1.25V. Nevertheless, the VCO was designed for a centre frequency of 5.1 GHz at 1.25V and it was accepted that the tuning range will not be symmetric about 5.1 GHz.

The final varactor capacitance (the final value of N_a) needed for a 5.1 GHz centre frequency depends not only the differential tank inductance but also the capacitance from the cross-coupled pair. The capacitance contributed by the cross-coupled pair depends on the final device size (number of fingers, bf and emitter length, el) and bias current (I_{tail}). The device size and bias current are primarily selected for low phase noise, and therefore, for each combination of these parameters considered, N_a is optimized to return the oscillation centre frequency back to 5.1 GHz (see Section 4.1.6).

4.1.6 Optimum Bias Current and Transistor Size for Low Phase Noise

Combining the initial cross-coupled pair with the differential inductor and the varactor selected in the previous two sections results in a VCO that will oscillate at about 5.1 GHz. This VCO, however, is not optimized for low phase noise. For each device size, there exists an optimum bias current that achieves the lowest phase noise for that device size, and when these results are compared, there exists an optimum device size (with an optimum bias) for the lowest VCO phase noise. Therefore, the lowest phase noise for each device size is found by sweeping I_{tail} for each size. Then the device size with the best phase noise is selected along with its associated optimum I_{tail}.

Thus oscillator phase noise was simulated as a function of I_{tail} for device sizes varying from small to large in total emitter length steps of approximately 10 μm (always with largest number if base fingers when more than one device configuration is possible). These device sizes, in increasing order, are: 2×5.1μm, 3×6.7μm, 3×9.9μm, 4×9.9μm, 4×20.3μm, 5×9.9μm, 5×12.3μm, 5×13.9μm and 5×20.3μm.

For each device size and I_{tail} combination, the varactor N_a is optimized for an oscillation frequency close to 5.1 GHz so that the size and current combinations can be accurately compared for phase noise at the same oscillation frequency. Since the number of varactor fingers N_a is an integer, the discrete optimizer in ADS is used (N_a step of 1) which can check the entire range of N_a. For a quicker simulation, the range of possible N_a was reduced by selecting the minimum N_a for f_o 5.1 GHz with the lowest current and smallest device and by selecting the maximum N_a for f_o 5.1 GHz with the highest current and the largest device. The optimizer range for N_a is then set to two below this minimum and two above the maximum resulting in far less iterations to achieve a 5.1 GHz oscillation frequency with the specific device size and bias current combination.

In summary, for each combination of bias current and device size, the varactor size is adjusted for an oscillation frequency of between 5.05 and 5.15 GHz and then the VCO is simulated for phase noise. These results are shown in Figure 45 and Figure 46.

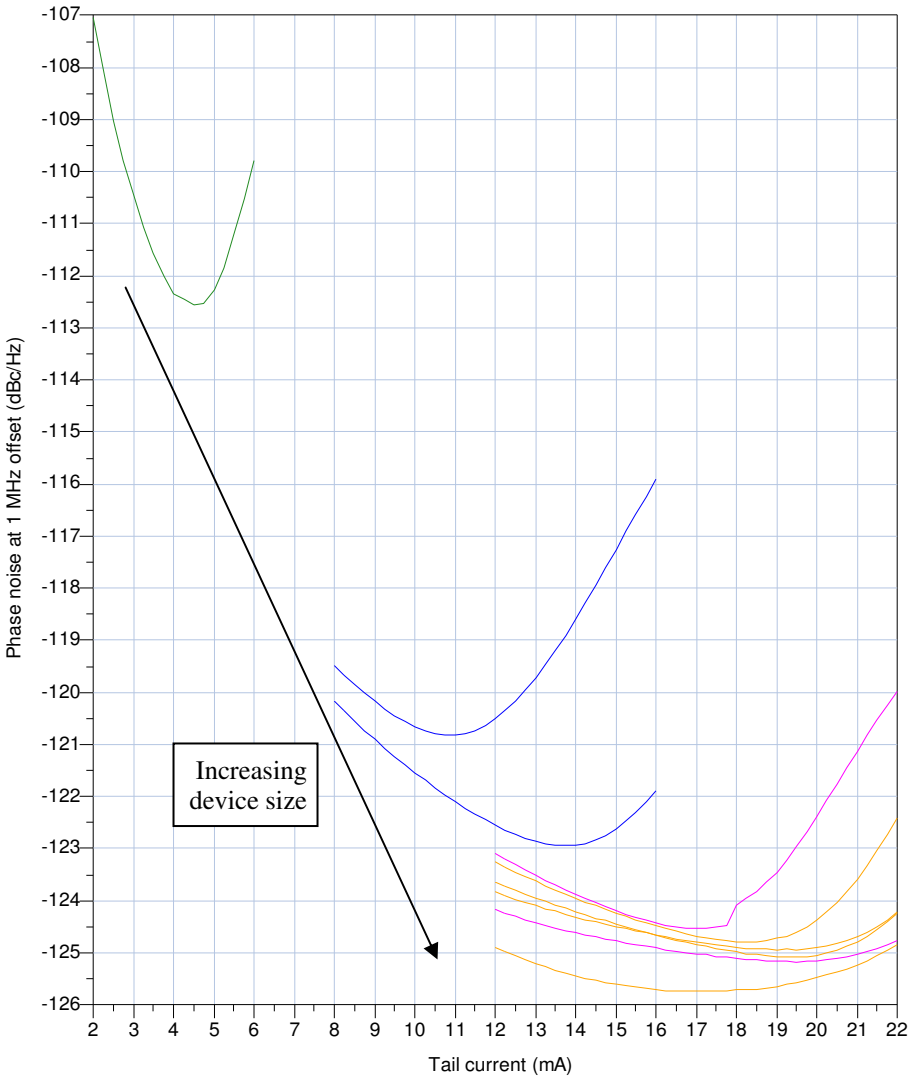


Figure 45: Simulated VCO phase noise v. device size and tail current

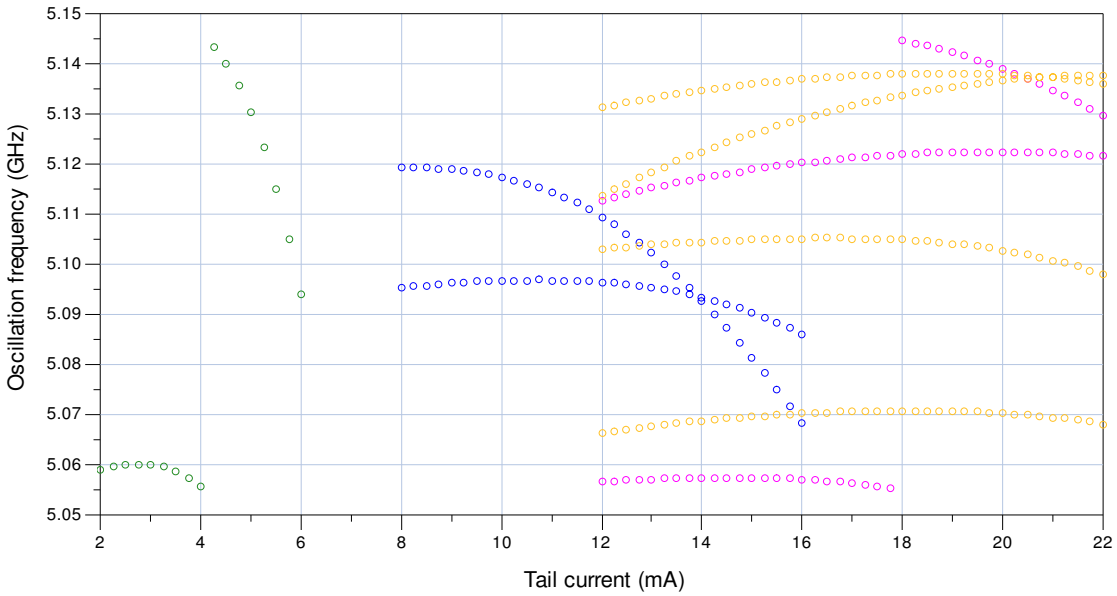


Figure 46: Simulated oscillation frequency for each point in Figure 45

Results in Figure 45 confirm that, as device size increases, the rate of improved phase noise slows and eventually, after 4×9.9 µm, any further size increase does not improve phase noise (but will reduce tuning range). Based on only this criteria a device size of 4×9.9 µm should be selected; however, further increasing size will increase the small-signal loop gain (SSLG) and hence the VCO will have safer start-up, although the frequency where the small-signal negative resistance becomes positive is lower for 5×20.3 µm (19 GHz) than for 4×9.9 µm (22 GHz) but these are both much higher than the tuning range. Further simulations of 4×9.9 µm versus 5×20.3 µm gives a SSLG of 1.091 versus 1.129 (both I_{tail} 15 mA but N_a 26 versus 23) and a tuning range of 1.476 versus 1.352 GHz. Since I_{tail} is the same, and for this design tuning range is not important but start-up is, a device size of 5×20.3 µm was chosen with I_{tail}=15 mA. Note that 15 mA is the point just about at the minimum phase noise, that is where the curve flattens, and the absolute minimum phase noise point is only just slightly lower but requires at least 2 mA more – not a great trade-off. So 15 mA represents the lowest current for approximately minimum phase noise.

A bias current of 15 mA can be handled by a 50 Ω thin film microstrip (TFMS) interconnect, however, depending on the metal layers used, a specific number of vias may be needed to handle this current density.

The simulated results of the VCO with cross-coupled 5×20.3 µm devices, I_{tail}=15 mA and N_a=23 results in a simulated centre frequency of f_o=5.126 GHz. This is shown in the simulated spectrum of Figure 47. The simulated phase noise is -125.6 dBc/Hz at an offset of 1 MHz and this is shown in Figure 48.

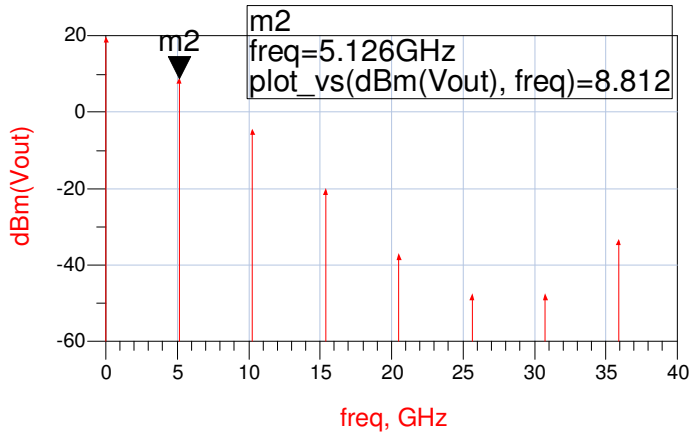


Figure 47: Simulated VCO spectrum at optimum phase noise

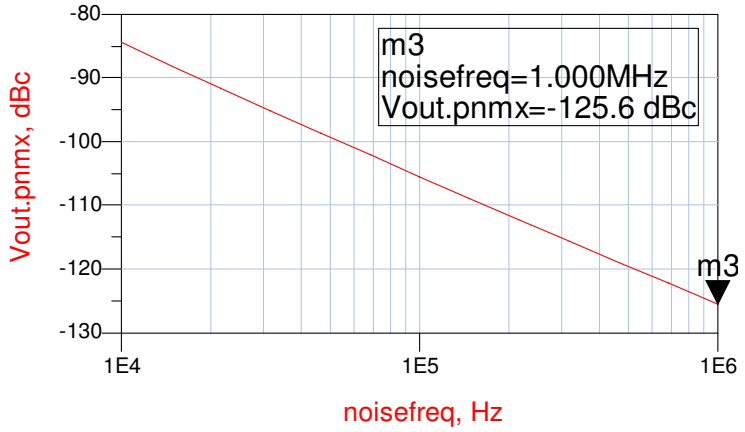


Figure 48: Simulated optimum phase noise at carrier offsets from 10 kHz to 1 MHz

4.1.7 Current Source with Noise Filtering

A simple current mirror is using a V_{cm}=3V supply generates the bias current, I_{tail}. A large device size (5×20.3 µm) was selected for a low base resistance noise (this noise will increase the oscillator phase noise) and for high current handling.

A low value unsalcided poly resistor was selected, which required a minimum width to handle the 15 mA of bias current. The actual width used was larger than this minimum, however, so that the bias current can be safely increased to as much as 24 mA in the lab during testing. For 15 mA with V_{cm}=3V and V_{be} 0.904V, then the current mirror resistor is approximately 140 Ω which, when realized as a low value unsalcided poly resistor, is 30 µm wide and 40 µm long.

The current source was simulated on its own using ADS. When the simulated reference current was generated using the 140 Ω poly resistor and a 3V supply, the simulated I_{tail} was 14.84 mA.

In order to add the current source to the VCO design, DC voltages V_b, V_c and V_{tune} must be increased by 1V to add headroom for the current source. The simulated centre frequency of the VCO does not change with the addition of the designed current source generating I_{tail}. The phase noise, however, is worse due to the added noise from the transistors in the current source. The simulated spectrum and phase noise of the VCO with the current source are shown in Figure 49 and Figure 50.

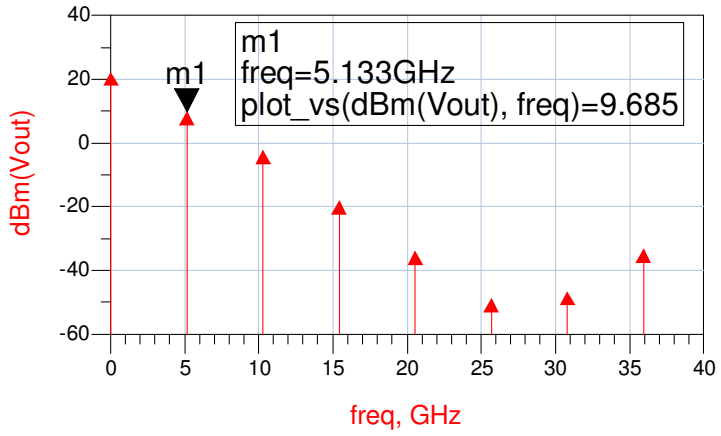


Figure 49: Simulated VCO spectrum with a current source generating I_{tail}

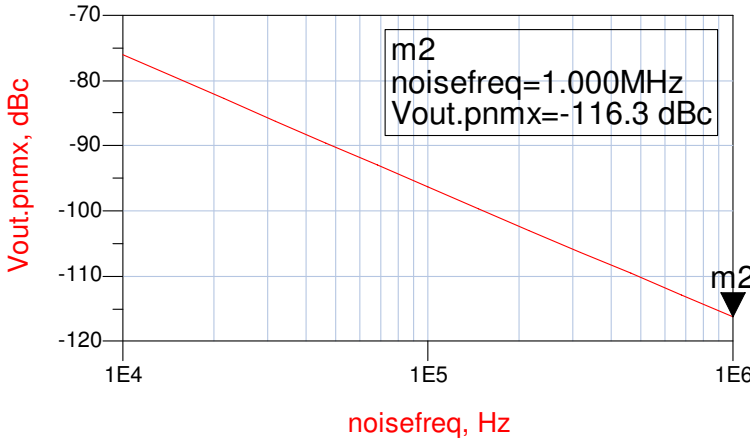


Figure 50: Simulated VCO phase noise with a current source generating I_{tail}

The degradation of the oscillator phase noise by 9 dB due to the current source can be avoided by using noise filtering. A large capacitor (2.741 pF) and a large inductor (2.377 nH) are used to prevent noise from the current mirror at the 2nd harmonic from entering the VCO differential pair. This filtering does not impact the DC bias current. Note that the self-resonant frequencies of the large capacitor and inductor elements were selected so that they do not vary significantly with frequency at the 2nd harmonic.

The simulated VCO performance with current mirror filtering lowers the phase noise to -123 dBc/Hz, which is very close to what it was before the current source was added. This simulated performance is shown in Figure 51 and Figure 52. These results demonstrate that the noise filtering minimizes the impact of the current source on the VCO phase noise.

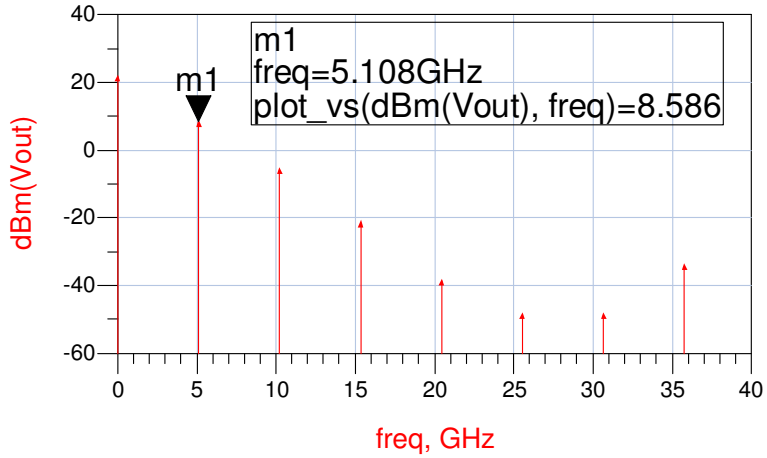


Figure 51: Simulated VCO spectrum with noise filtering in the current source

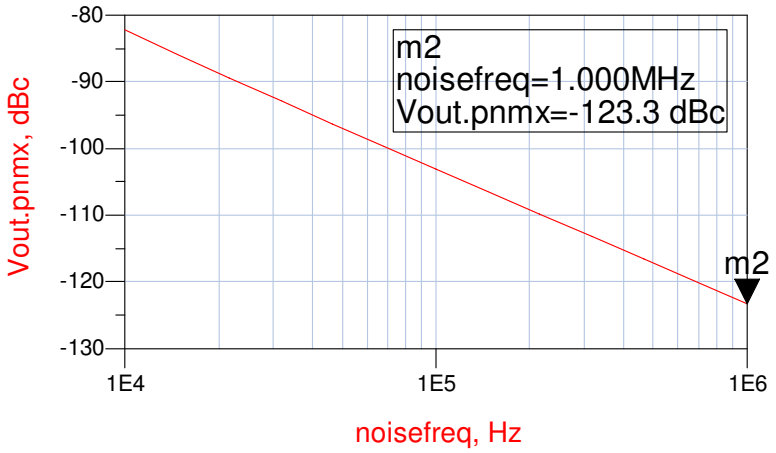


Figure 52: Simulated VCO phase noise with noise filtering in the current source

4.1.8 Oscillator Start-Up

The VCO small-signal loop gain was simulated, as shown in Figure 53, to confirm the small signal loop gain was greater than 1 and hence guarantee oscillator start-up. Since the simulated small-signal loop phase was zero at 4.3 GHz, this is the initial oscillation frequency although as the oscillator signal grows and the oscillator becomes nonlinear the oscillator frequency changes to the desired 5.1 GHz as predicted by the earlier steady-state harmonic balance simulations. Envelope simulation in ADS also confirmed that the conditions are suitable for start-up. This is shown in Figure 54.

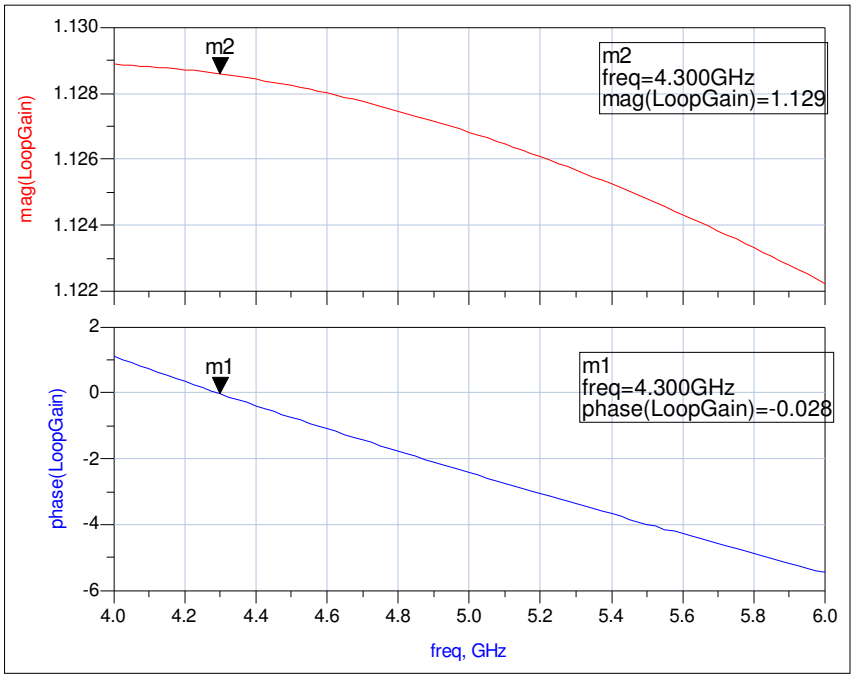


Figure 53: Simulated small signal loop gain that demonstrates VCO start-up

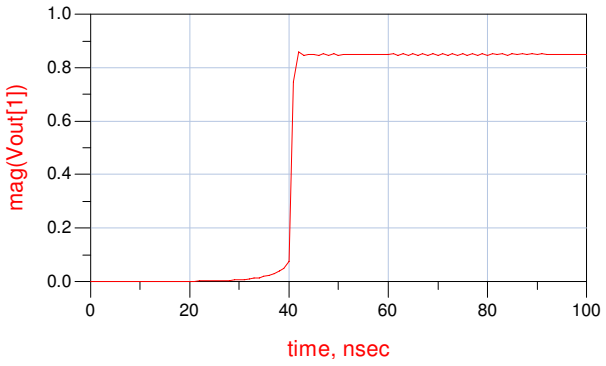


Figure 54: VCO start-up using envelope simulation

4.1.9 Buffer Amplifiers

Two common collector buffer amplifiers are used to connect each differential oscillator output to a 50 Ω load without loading the oscillator (since the common collector amplifiers have high input impedances). The gain of these amplifiers is less than one, so there is some loss of the signal. The buffers also distort the signal a little. Nevertheless, buffers are one of the most commonly used methods to match an oscillator to a 50 Ω load.

The voltage gain of a common collector amplifier with $R_L = \infty$ is A_v 1 (this is the open-circuit voltage gain). When the same amplifier is connected to a real load with $R_L \neq \infty$, then A_v is reduced

by the factor $R_L/(R_L+R_o)$, where R_o is the output resistance of the common collector amplifier. But, if $R_o<<R_L$ then $R_L/(R_L+R_o)$ 1 so that voltage gain is not only independent of the load but is the same as if the load was infinite, that is A_v 1. Therefore a large NPN device size was chosen for each buffer so the output resistance is small and hence the voltage gain is close to one and relatively independent of the load (and thus requires no matching).

The buffers use large capacitors and inductors for the blocking and choke elements. Thus a 2.741 pF capacitor and a 2.377 nH single-ended inductor were used, each having parameters of 50 50 µm, $R_{5.1GHz}$=0.056 Ω, SRF 18 GHz and x = y = 100 µm, w=2.6 µm, s=3 µm, n=6.5, $R_{S,\ 5.1GHz}$=13.78 Ω, SRF>23 GHz, respectively.

The emitter is biased at -3V so that the collector can be both DC and RF ground (and thus no elements are required). The base is therefore also biased at negative potential, and it is swept to find the optimum bias for the lowest output resistance (causing voltage gain as close as possible to one). This can be approximated using small signal simulation; however, large signal simulation is more accurate since each amplifier operates at large signal. ADS includes two ways to simulate large signal performance: large signal s-parameter (LSSP) simulation and harmonic balance (HB) simulation. The LSSP simulation showed that the input resistance drops to a minimum (with reactance maximized) around V_b=-1.95V and then rises (and reactance drops); however, the output resistance reaches minimum around V_b=-1.95 V and does not rise (and the output reactance is almost negligible). The HB simulations showed that A_v increases towards 1 and starts to saturate around -1.95V. Therefore, as base bias increases, the output resistance decreases with V_b=-1.95V being optimal, while at the same time input resistance is minimized and the reactance is maximized.

The buffer, combined with the VCO, was then simulated. The common collector base bias was swept to refine the base bias for a buffer gain, A_v, close to one (buffer gain is $A_v=V_{load}/V_{out}$, where V_{out} is the oscillator output voltage or buffer input voltage and V_{load} is the buffer output voltage). The base voltage was varied from -2.2 to -1.8V (V_{BE} from 0.8 to 1.2V) and the simulated result is shown in Figure 55.

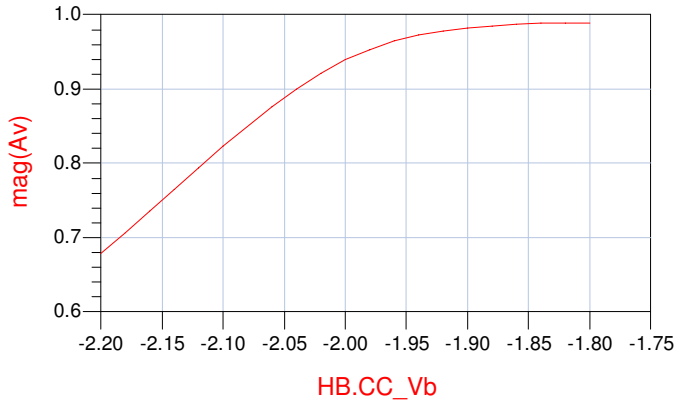


Figure 55: Simulated buffer gain, A_v, versus buffer base bias, V_b

Once again, -1.95V is the point where A_v starts to flatten in Figure 55, and hence also where the output power from the buffer is closest to that of the oscillator. Therefore, the common collector buffer base bias V_b was chosen to be -1.95V.

Comparing the power at the input of the buffer (output of the oscillator core) to the output of the buffer also confirms that -1.95V base bias is the point where the buffer does not load the oscillator. This is shown in Figure 56.

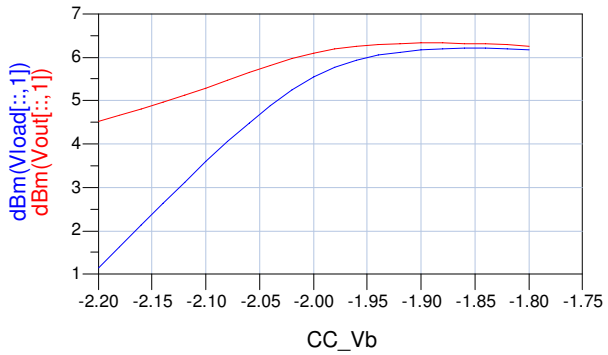


Figure 56: Simulated buffer input and output power versus buffer base bias

Simulations of the entire VCO with the two buffers result in an oscillation frequency of 5.217 GHz with output power of 5.992 dBm into a 50 Ω load. The spectrum of the signal at the input of the buffer is shown in Figure 57 and at the output of the buffer in Figure 58. The buffer voltage gain is 0.967. Phase noise at 1 MHz offset is -122.2 dBc/Hz, as shown in Figure 59. The VCO with the buffers produces two differential output signals, as shown in Figure 60.

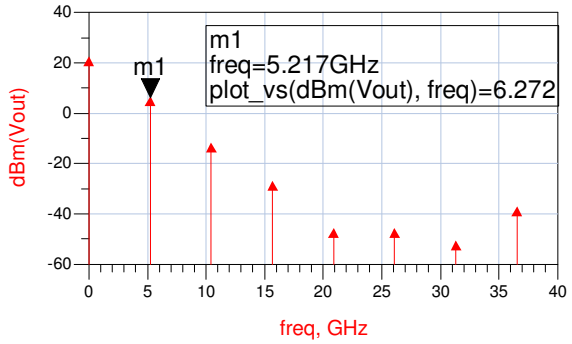


Figure 57: Simulated spectrum at the input of the buffer

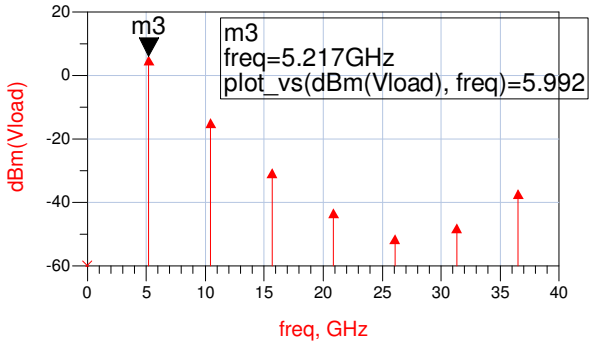


Figure 58: Simulated spectrum at the output of the buffer, which is also the output of the VCO

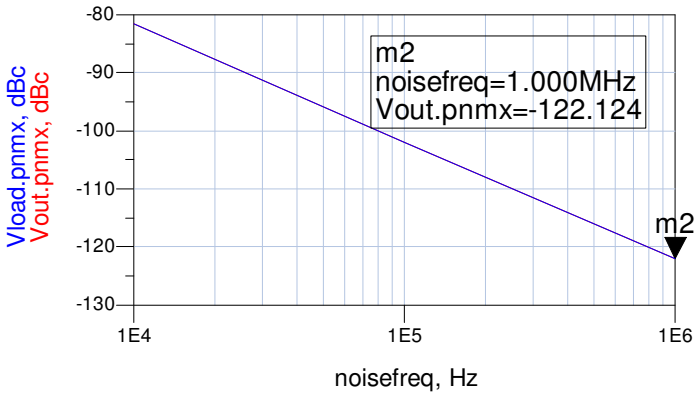


Figure 59: Simulated phase noise of the VCO, with buffer amplifiers, taken at the input (blue) and output (red) of the buffers (and showing the same phase noise at both locations)

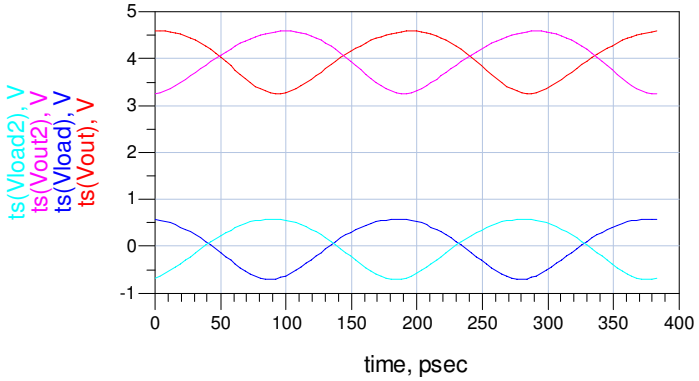


Figure 60: Simulated differential output voltage (one from each buffer)

4.1.10 Interconnects

The lumped elements and transistors were interconnected using 50 Ω thin film microstrip (TFMS) lines. The design uses TFMS with the signal line on the top metal layer and the ground on the bottom metal layer. The maximum ground plane width is limited to avoid the need for stress relief slits. The ground plane is solely used under the interconnecting TFMS lines; there is no ground plane under the lumped elements nor within 10 µm of any lumped element because the lumped element models from the foundry do not include a ground plane.

The TFMS interconnects are simulated using the MLIN element in Agilent ADS. Momentum electromagnetic simulations were not performed. Parasitic extraction was also not performed, although a capacitor was included in ADS to account for the coupling of the TFMS cross-over in the cross-coupled pair.

The VCO was simulated after interconnects were added; however, their impact was minimal.

4.1.11 Fabrication of the VCO

The VCO, with buffers and the current source, was fabricated by the foundry. A photograph of the completed circuit is shown in Figure 61.

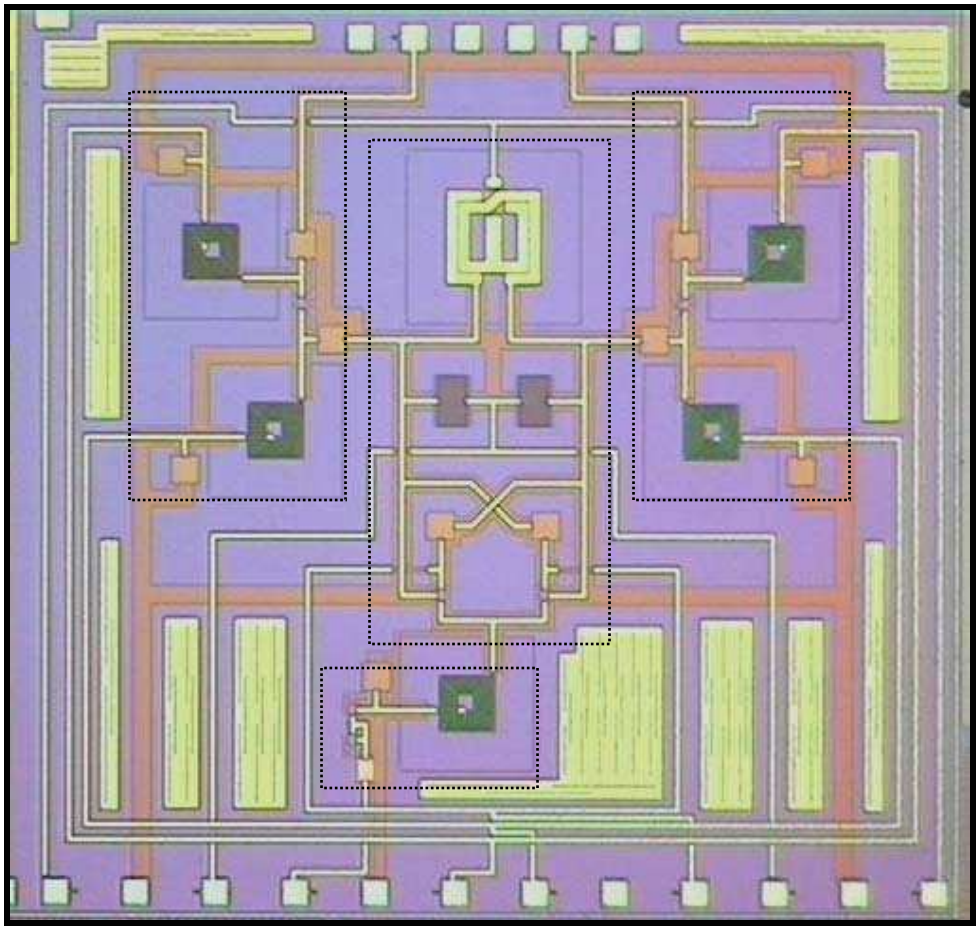


Figure 61: Photograph of the fabricated VCO (centre), two buffer amplifiers (far left and right) and a current source with noise filtering (bottom)

4.1.12 VCO Measured Performance

The VCO was measured on-wafer using a spectrum analyzer. The oscillation frequency was 5.1005 GHz with 5 dBm output power as shown in Figure 62. The spectrum was measured to the fifth harmonic, as shown in Figure 63, showing no spurious frequencies. The bias conditions for these measurements were: V_c = 4V, V_{cm} = 3.5V, V_{bb} = -1.95V, V_{ee} = -3V, V_b = 2V and V_{tune} = 7.5V. This bias condition is slightly different than the design bias with both V_{tune} and V_{cm} being slightly higher to increase the measured frequency and power to 5.1 GHz and 5 dBm.

The loss in the cabling was estimated to be 2.2 dB, and this loss has been removed from the measured data.

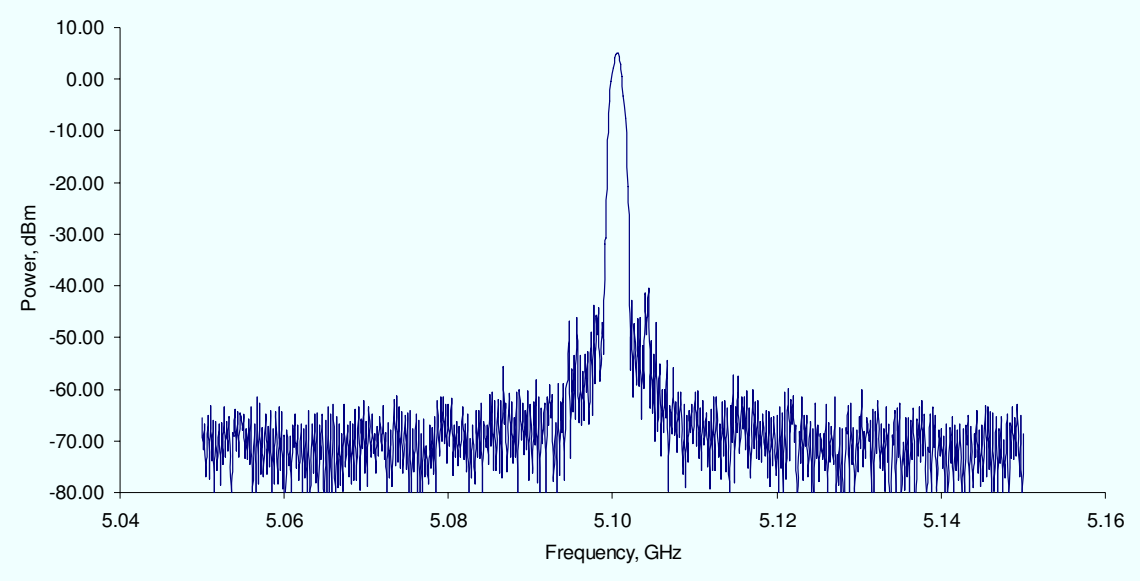


Figure 62: Measured VCO spectrum

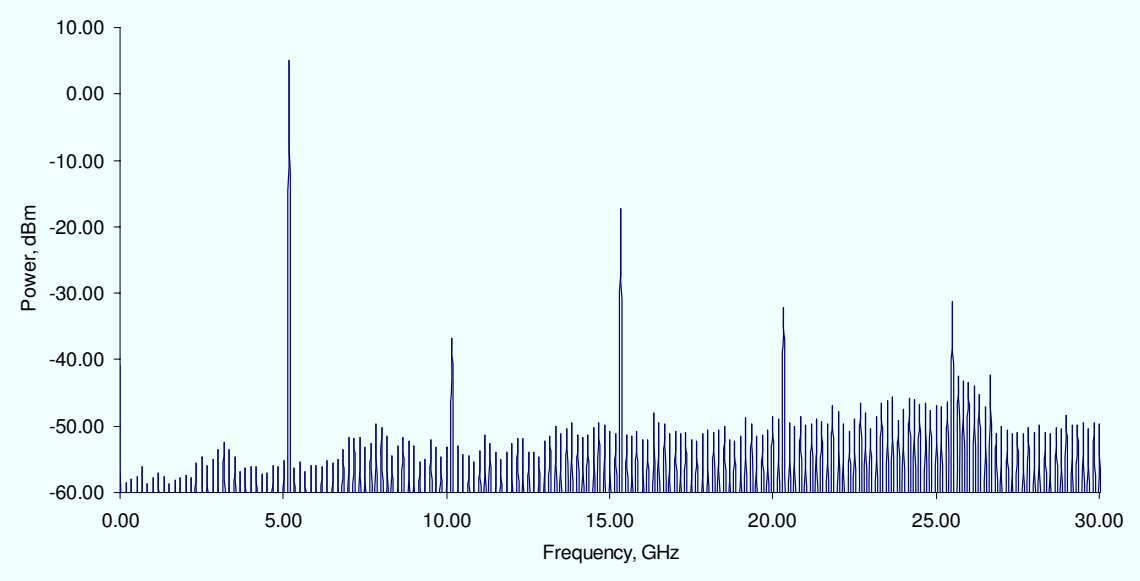


Figure 63: Measured VCO harmonics

The measured oscillator tuning range is shown in Figure 64. Since only V_{tune} is varied, the output power varied also. When V_{tune} and V_{cm} were tuned simultaneously, then constant output power was achieved over the tuning range. This is shown in Figure 65.

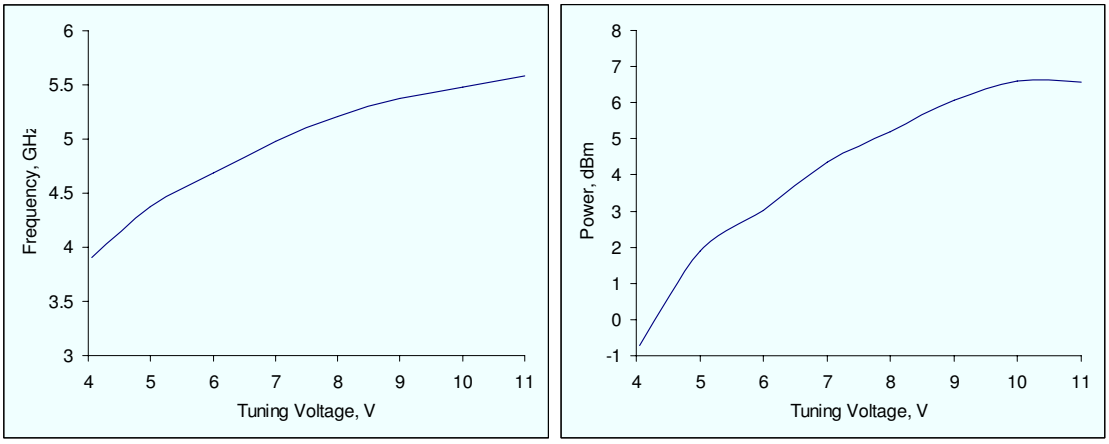


Figure 64: Measured VCO tuning range by changing tuning voltage only

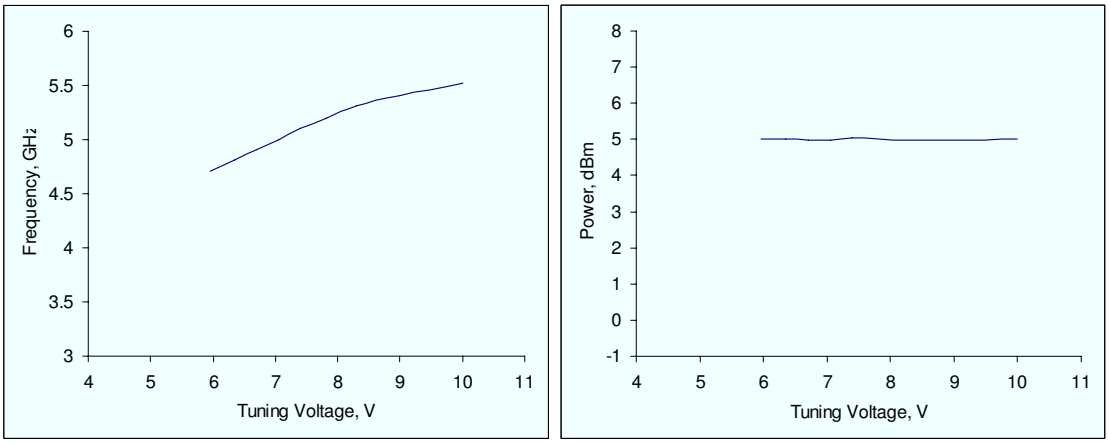


Figure 65: Measured VCO tuning range by changing tuning voltage and bias current simultaneously

The phase noise, shown in Figure 66, was measured using an Agilent E5052B Signal Source Analyzer (SSA) and found to be -50, -84 and -112 dBc/Hz at offsets of 10 kHz, 100 kHz and 1 MHz, respectively. The increase in phase noise at offsets higher than 1 MHz is due to noise in the bias supply. This was confirmed by using the SSA to measure the noise of the baseband supply and overlaying this on the phase noise of the VCO. This is shown in Figure 67 where the blue is the phase noise of the bias supply and the yellow is the phase noise of the VCO.

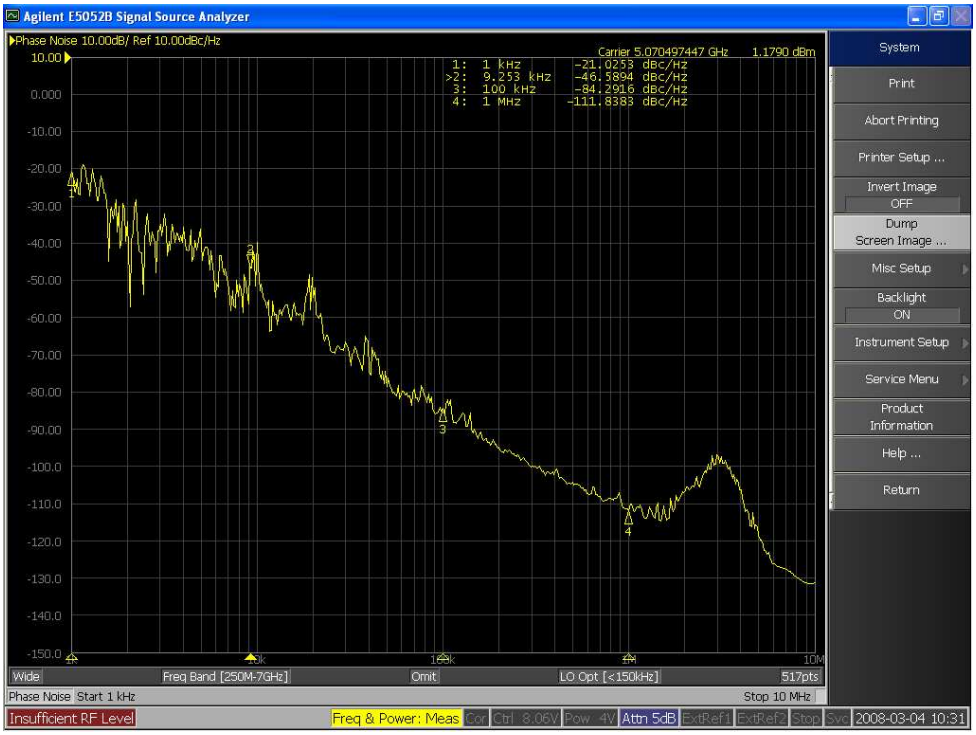


Figure 66: Measured oscillator phase noise

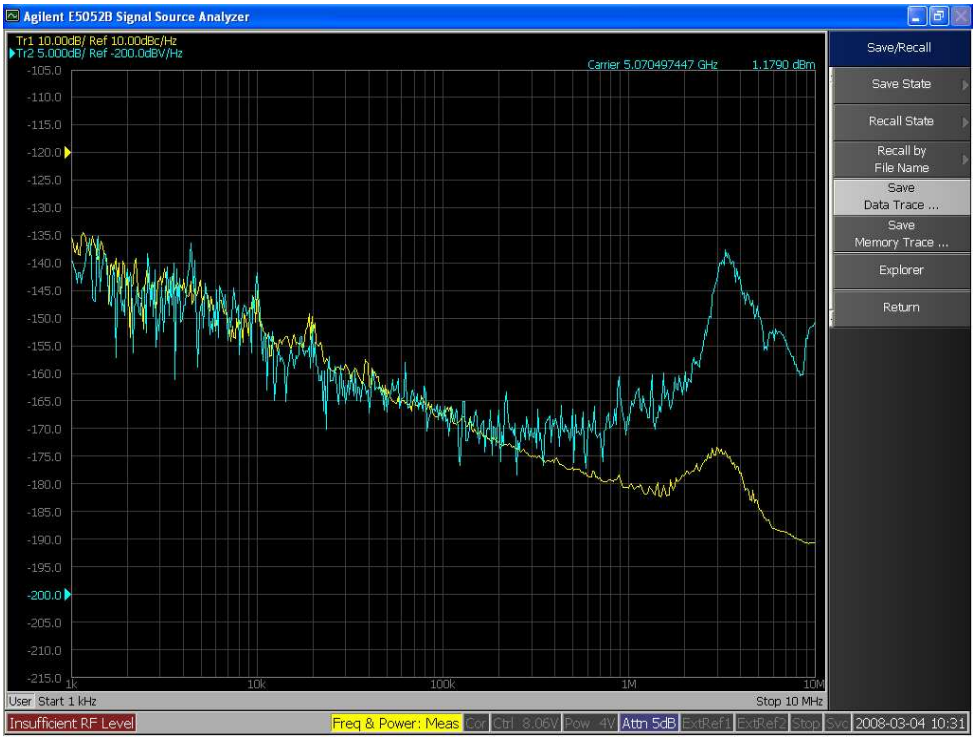


Figure 67: Measured phase noise of the VCO (yellow) compared to the measured phase noise of the bias supply (blue)

4.2 Gilbert Cell Mixer at 5 GHz

4.2.1 Introduction

The purpose of a mixer is to convert a signal from one frequency to another. A mixer can up-convert or down-convert a signal to higher or lower frequencies respectively. In this design, a down conversion mixer is considered where a radio frequency (RF) signal is multiplied by a local oscillator (LO) at the input to the mixer to be down converted to an intermediate frequency (IF) signal.

4.2.2 Basic Concepts

There are different mixer topologies and they can be separated into two kinds: active and passive mixers. Active mixers have an associated gain whereas passive mixers can achieve at best a gain of one. Active mixers are also divided further to single-ended and differential implementations. Differential implementations are preferred due to their superior ability to cancel undesired noise. Finally the differential mixer implementations are categorized as single and double balanced configurations as shown in Figure 68. Double balanced mixers, also called Gilbert cell mixers, are preferred over the single-balanced implementations as the Gilbert cell suppresses the LO-to-IF and RF-to-IF feed through, which can increase linearity and decrease susceptibility to supply voltage noise.

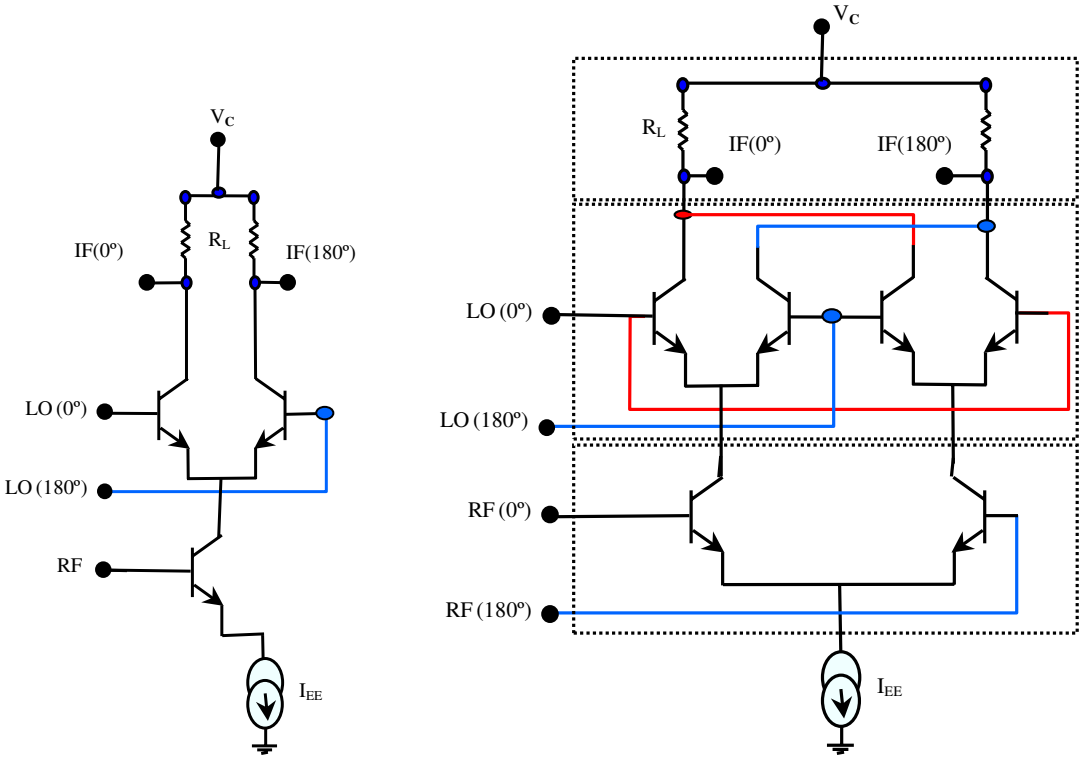


Figure 68: (a) Single-balanced mixer, (b) Double-balanced mixer (Gilbert Cell)

Mixers work on the basis of a trigonometric identity with two signals multiplied together as shown in equation (1):

$$(A\cos\omega_1 t)(B\cos\omega_2 t) = \frac{AB}{2}\left[\cos(\omega_1+\omega_2)t + \cos(\omega_1-\omega_2)t\right] \quad (1)$$

The concept of mixing is more fully illustrated in Figure 69. If two signals with frequency-dependent components $f(\omega_1 t)$ and $f(\omega_2 t)$ are applied to a mixer, the output signal will be composed of a sum of mixing products. Considering only the second order (additional products are usually filtered out) the IF signal would be composed of the sum $f(\omega_1+\omega_2)t$ and difference $f(\omega_1-\omega_2)t$ of the input frequencies.

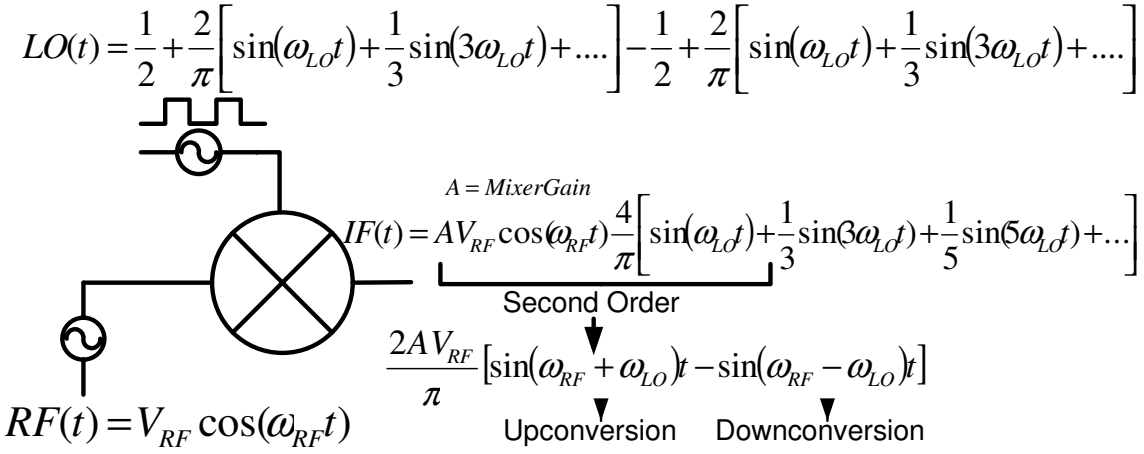


Figure 69: Mixer representation

In real implementations, the LO input signal is a square wave due to its preferred abrupt switching that improves noise performance. In the simulations for this design, however, a sinusoidal LO signal can be used because a sinusoidal signal at high frequencies has a very steep slope, closely resembling a square wave signal.

4.2.3 Proposed Mixer

The mixer topology for this design is the double balanced mixer with series resistors and current bleeding transistors shown in Figure 70. The degenerative resistors (R_E) improve linearity with the cost of reduced conversion gain. The current bleeding transistors reduce the current in the LO transistors while still delivering the required current to the RF stage. Reducing the current through the LO transistors improves noise performance and conversion gain. A tail current (I_{EE}) of 3 mA is selected for low power consumption.

The specifications for the mixer design are:

Input signal RF frequency: 4.9 GHz

Intermediate frequency (IF): 200MHz

Mixer SSB noise figure: ≤ 10 dB

Mixer IIP3: ≥ 6 dBm

1dB compression: ≥ -20 dBm

Supply voltage: 3 V

Mixer conversion gain: ≥ 10 dB

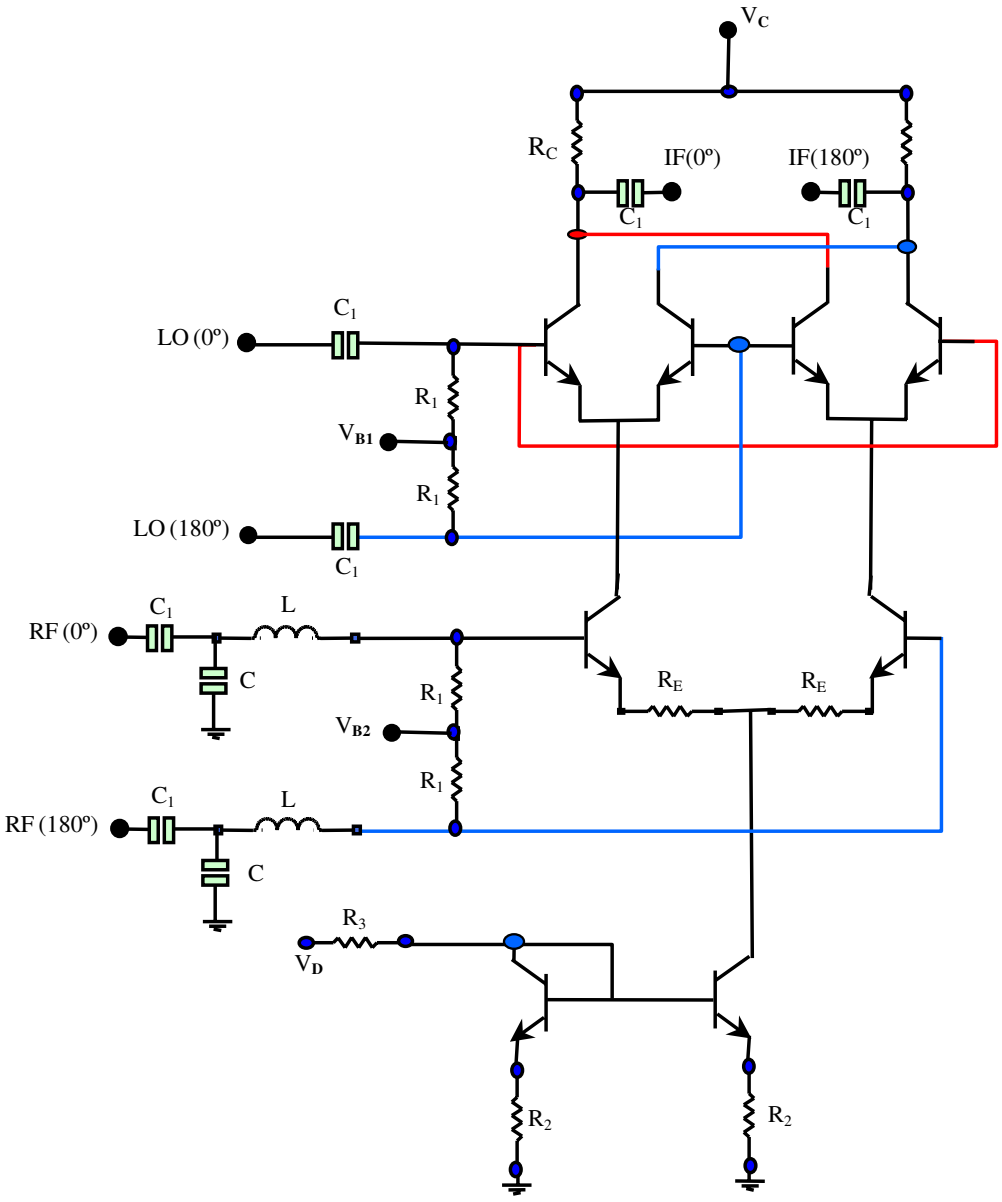


Figure 70: Proposed mixer implementation

4.2.4 Mixer Design

4.2.4.1 Transistor Sizing

The switching upper-quad LO transistors are sized to operate close to their peak f_T and to handle the current which passes through RF transistors. For these transistors the emitter length and width are 3.5 µm and 0.3 µm, respectively, and their f_T is above 60 GHz, as shown in Figure 71.

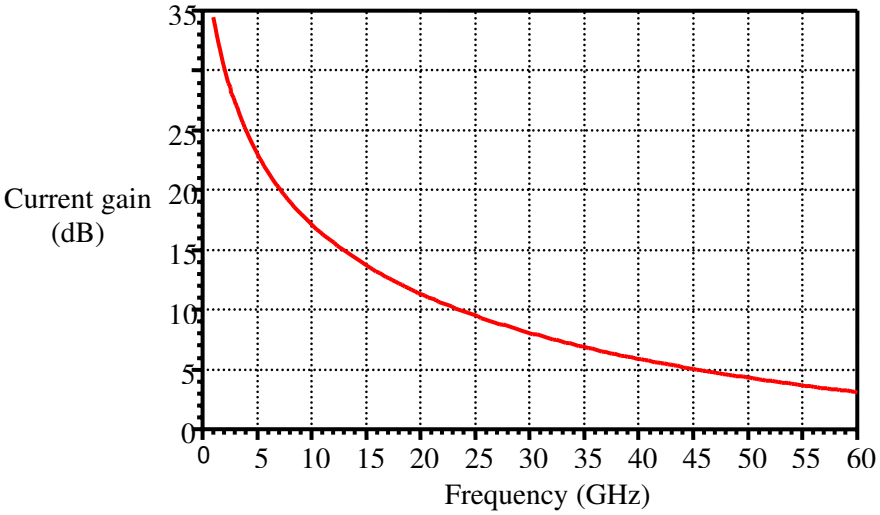


Figure 71: Switching transistor characterization - simulated f_T

The RF stage transistors are sized so that the particular bias current running through them ensures minimum noise figure. The transistor dimensions that correspond to this condition were an emitter length of 13.9 µm and 3 base fingers. The noise characterization for the selected transistor is shown in Figure 72.

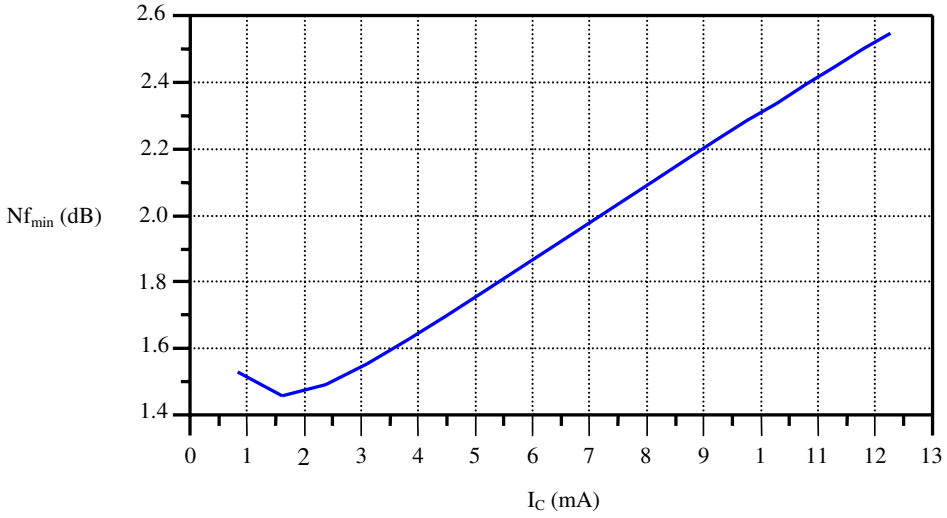


Figure 72: Simulated minimum noise figure

4.2.4.2 Picking the LO Level

The LO level was set to 300mV to saturate the upper-quad transistors. One of the negative consequences of choosing a relatively high LO level is increased LO feed-through. This issue was not critical since the LO and the IF are far apart in frequency and hence the LO can be easily filtered.

4.2.4.3 Degeneration and Load Resistances Selection

These two resistors are determined from linearity and gain requirements, with the observation that the degeneration resistor will have a major impact on the noise figure performance. The degeneration resistance R_E was selected as follows. From $P = \frac{Vrms^2}{R}$ an IIP3 of 6 dBm for a 100Ω differential circuit corresponds to a signal swing of V_{rms} = 0.632V, which is equivalent to 0.316V per side for the differential circuit. Therefore r_e = 17Ω from $r_e = \frac{1}{gm}$ where $gm = \frac{I_C}{V_T}$ and R_E = 83Ω using $R_E = 2\left[r_e \left(\frac{V_{ip}}{2V_T} \right)^{2/3} - r_e \right]$. Since the latter formula is an approximation and there are other nonlinearities, R_E = 90Ω was chosen. With r_e and R_E known, the load resistor R_C is found from gain $G = \frac{2}{\pi} R_c \frac{1}{r_e + \frac{R_E}{2}}$ noting that we want 10dB or 3.2 (v/v). This corresponds to R_C = 320Ω.

4.2.4.4 Mixer Biasing

In order to properly bias each transistor in the mixer, bias voltages of V_{BE} 0.85 – 0.9V and V_{CE} = 0.5 V need to be provided. This means a forward biased base-emitter junction and a slightly reversed biased base-collector junction (0.35-0.4V). All biasing resistors were selected to be R_1 = 5 kΩ in order to provide a high impedance to the RF and LO signals.

Also, a current mirror using a single transistor was selected, and therefore the degeneration resistor R_E was split in two equal components $R_E/2$. This causes an extra voltage drop across them (few tens of mV). Resistors to the ground in the current mirror, R_2, are used for thermal stability improvement.

Biasing conditions were achieved by employing two ideal voltages sources: V_{B1} = 2.1 V for LO quad and V_{B2} = 1.6V for the lower transistors (as current source and as reference for the current sink). All these sources can be easily implemented using resistor divider configurations. DC operating points are shown in Figure 73.

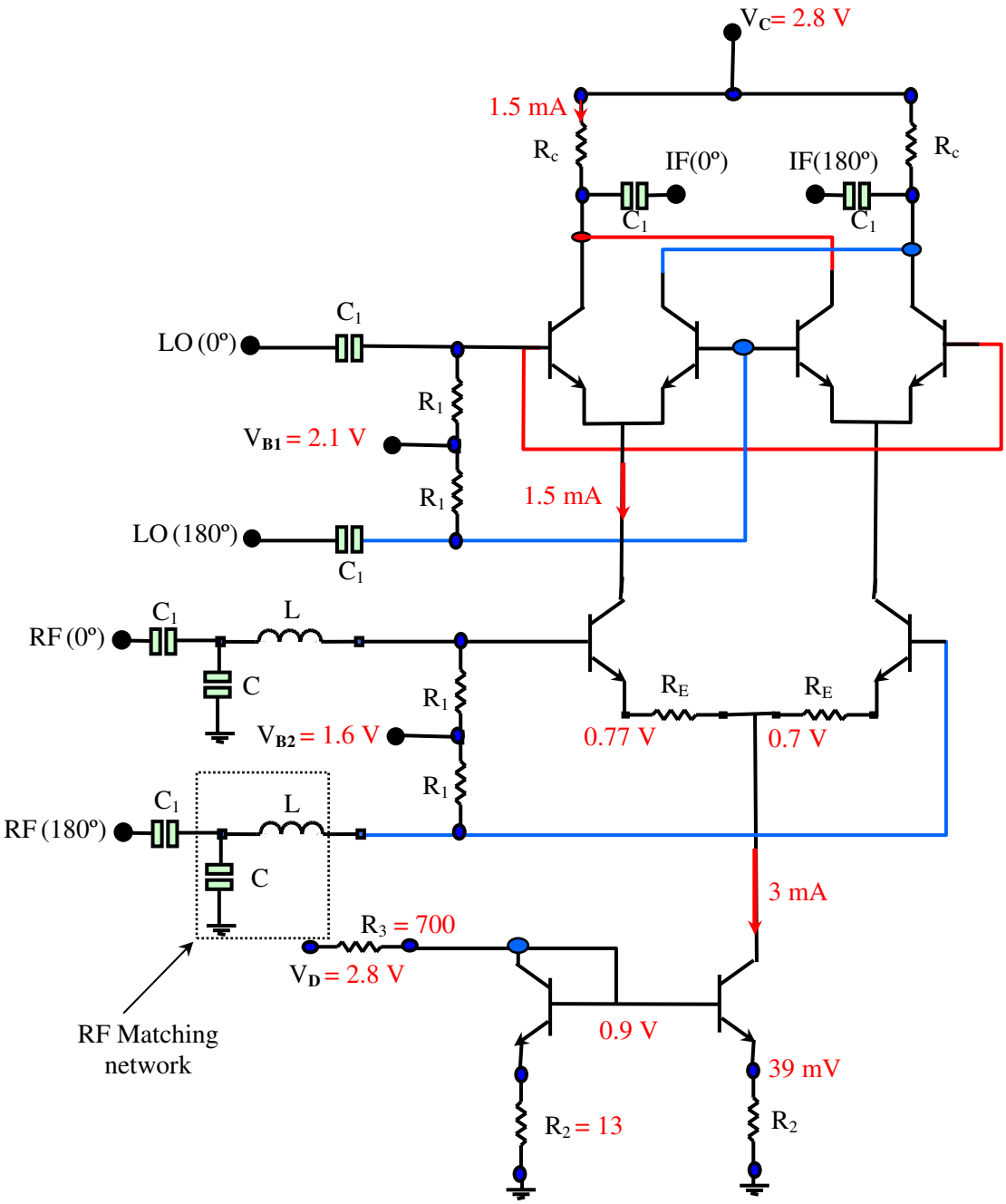


Figure 73: Voltage budget for the Gilbert Cell mixer

4.2.4.5 SSB Mixer Noise

The mixer SSB noise is calculated by using the results of (2) to (5) in (6). First, the noise spectral density produced by the resistance in the source, R_{match}, is:

$$V_{n,Source} = \sqrt{4KTR_{Match}} = \sqrt{4\times(4\times10^{-21})\times100} = 1.29\,{}^{nV}\!/_{\sqrt{Hz}} \tag{2}$$

The noise generated by R_{match} will be amplified by the mixer and passed to the mixer output:

$$V_{n0,Source} = \frac{V_{n,Source}}{2}A_v = \frac{1.29}{2}3.2 = 2.1\,{}^{nV}\!/_{\sqrt{Hz}} \tag{3}$$

At the same time, R_E will be a noise source, internal to the mixer producing a noise current $I_{n,RE}$ with following spectral density:

$$I_{n(R_E)} = \sqrt{{}^{4KT}\!/_{R_E}} = \sqrt{\frac{4\times(4\times10^{-21})}{90}} = 13.33\,{}^{pA}\!/_{\sqrt{Hz}} \tag{4}$$

Thus, the total noise at the output of the mixer is calculated with the following relation since the sources are uncorrelated:

$$V_{n0,Total} = \sqrt{{V_{n0,source}}^2 + {V_{n0,R_E}}^2} = 5.6\,{}^{nV}\!/_{\sqrt{Hz}} \tag{5}$$

The approximate noise figure is then given by:

$$NF = 20\log\left(\frac{\sqrt{2}\cdot V_{n0,total}}{V_{n0,source}}\right) = 11.5\,\text{dB} \tag{6}$$

4.2.4.6 Power Consumption

The current through each transistor of the RF pair was selected to be about 1.5mA for minimum noise. Therefore, the current through each of the two current sink transistors is about 3 mA and the current drawn from the 2.8 V power supply V_c is about 6 mA with P_{diss} = 15 mA.

4.2.5 Simulation Results

The circuit was simulated using the Agilent ADS simulator with a -30 dBm RF input power at 4900 MHz and a local oscillator frequency of 5100 MHz. The simulated IF output spectrum, shown in Figure 74, is free of spurious mixer products.

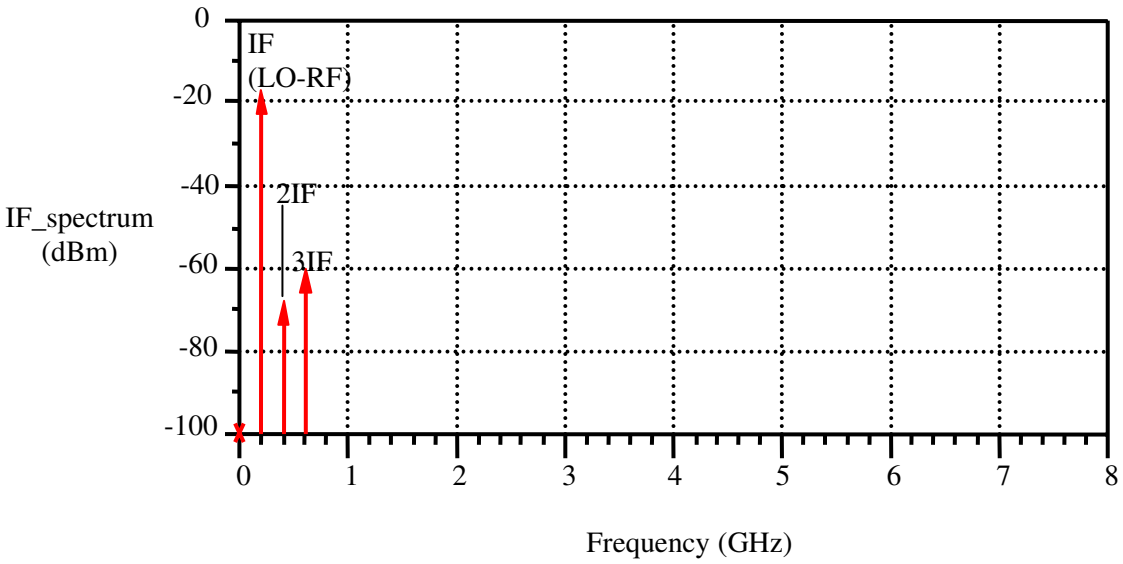


Figure 74: Simulated IF spectral output

Figure 75 shows the dependence of the conversion gain characteristics on LO input power for the Gilbert Cell mixer. The frequency is fixed at 5.1 GHz for the LO and 4.9 GHz for the -30 dBm RF signal. Input LO power impacts the conversion gain as illustrated in Figure 75 where the conversion gain is maximum for LO input power from 0 to 3 dBm. Figure 75 shows that an input LO power of around 3 dBm gives the highest simulated conversion gain; however, the input LO power also affects the noise figure. For this reason the optimal LO input power is chosen considering both the simulated conversion gain of Figure 75 and also the simulated noise figure shown in Figure 76. Figure 75 and Figure 76 show that the simulated gain and noise figure are both relatively flat for LO powers from -6 dBm to 4 dBm. Considering both the simulated conversion gain and the simulated noise figure, an optimal LO input power of 0dBm is observed.

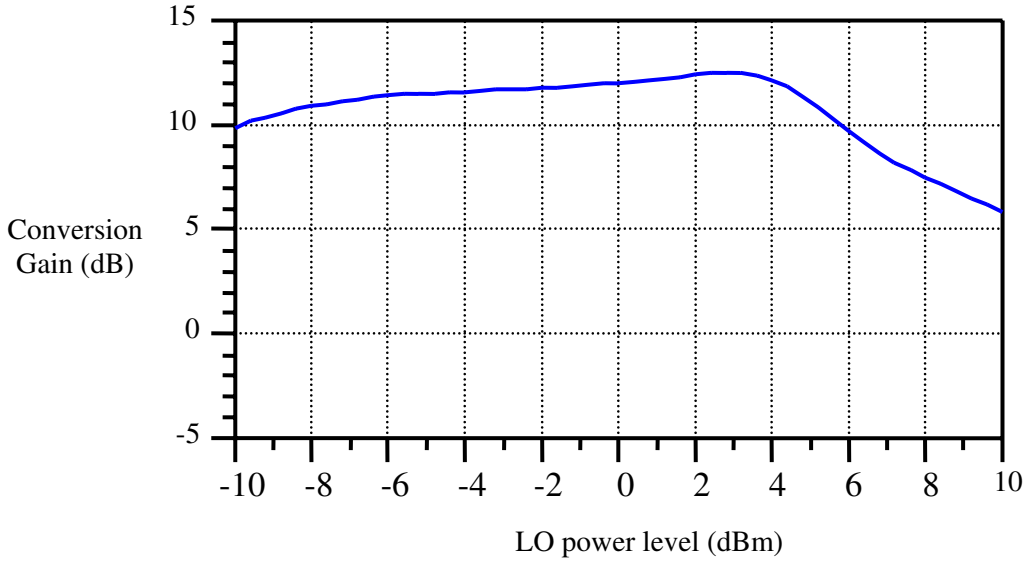


Figure 75: Simulated conversion gain versus LO input power

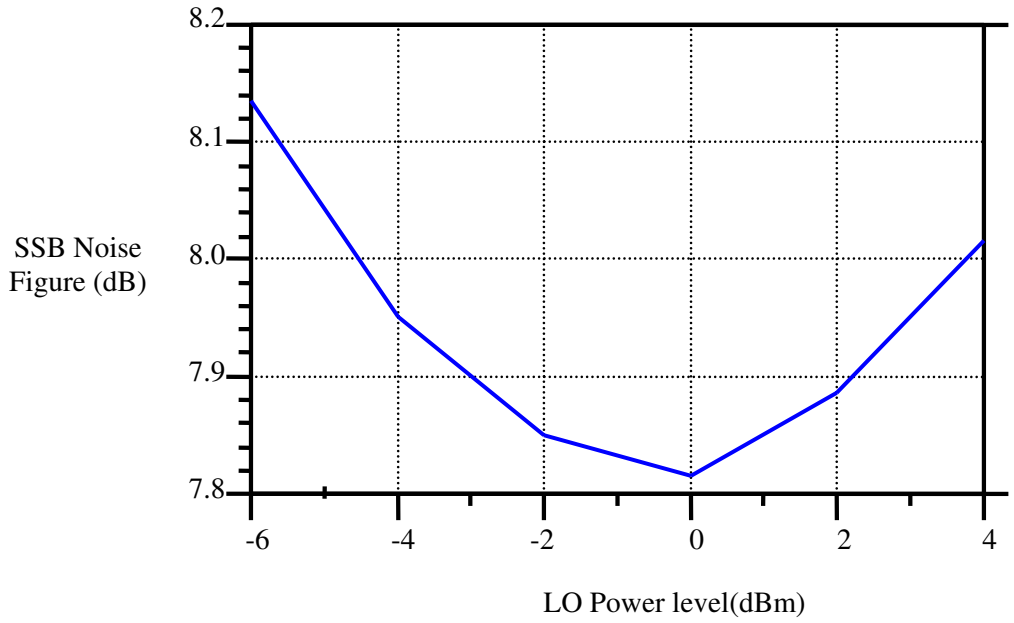


Figure 76: Simulated noise figure versus LO input power

The simulated conversion gain across the RF bandwidth of 3.5–5.5 GHz is 12.5 ± 0.3 dB, as illustrated in Figure 77. For this simulation, the IF was fixed at 200 MHz and the LO and RF input powers were set to 0 and -30 dBm, respectively.

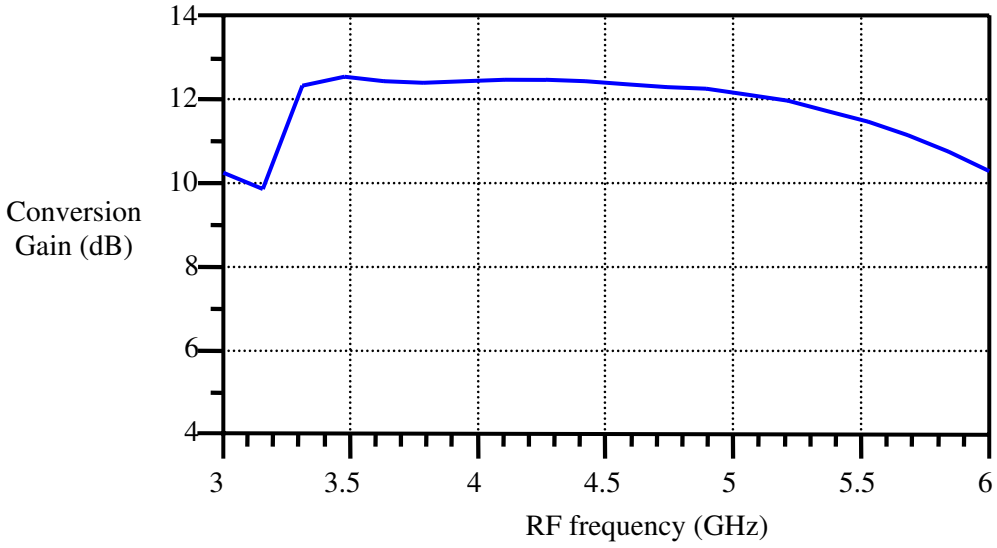


Figure 77: Simulated conversion gain versus RF frequency

Figure 78 shows that the simulated RF return loss is better than 10 dB over a 4.9 – 6 GHz frequency range. For this simulation, the IF was fixed at 200 MHz and the LO and RF input powers were set to 0 and -30 dBm, respectively.

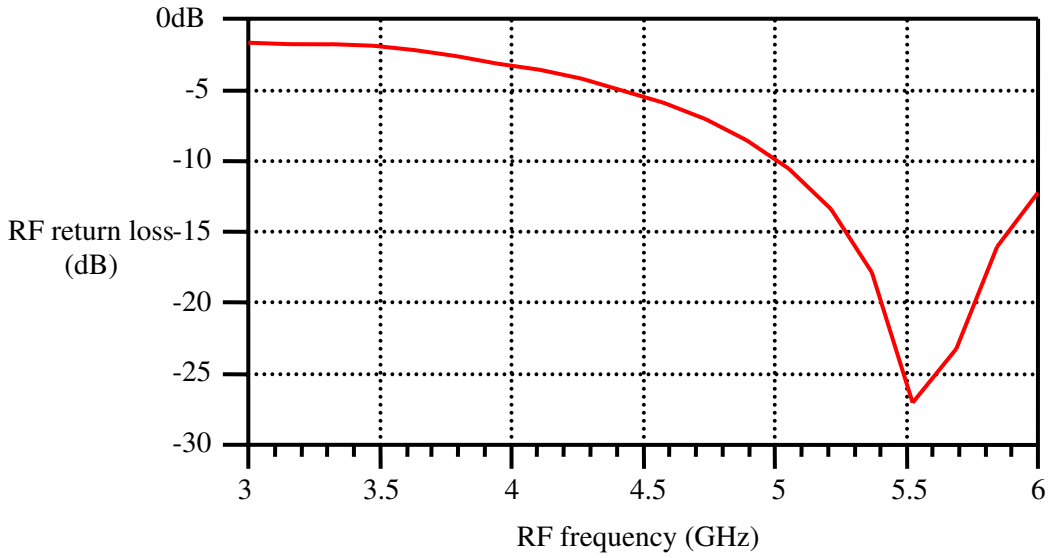


Figure 78: Simulated RF port return loss of the Gilbert Cell mixer

Figure 79 shows the simulated input/output characteristics at an LO input power of 0 dBm. The 1-dB compression point of the conversion gain is achieved with an RF input power of -20 dBm.

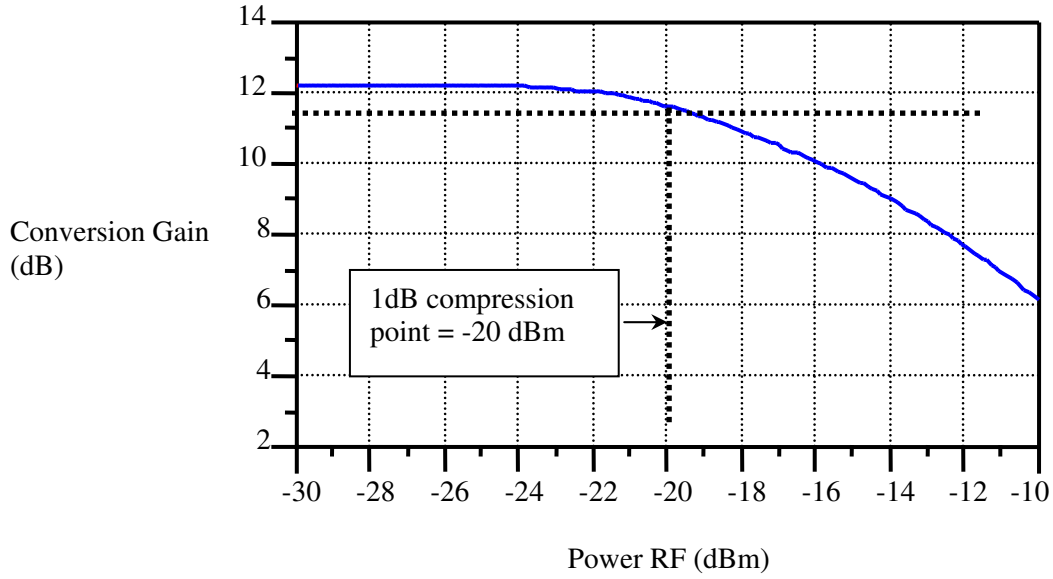


Figure 79: Simulated 1-dB compression point of the Gilbert Cell mixer

The simulated third-order intercept (IIP3) is -5.8 dBm as shown in Figure 80. This simulated result is quite different from the specification of 6 dBm; however, this may be due to the fact that the equation is only an approximation.

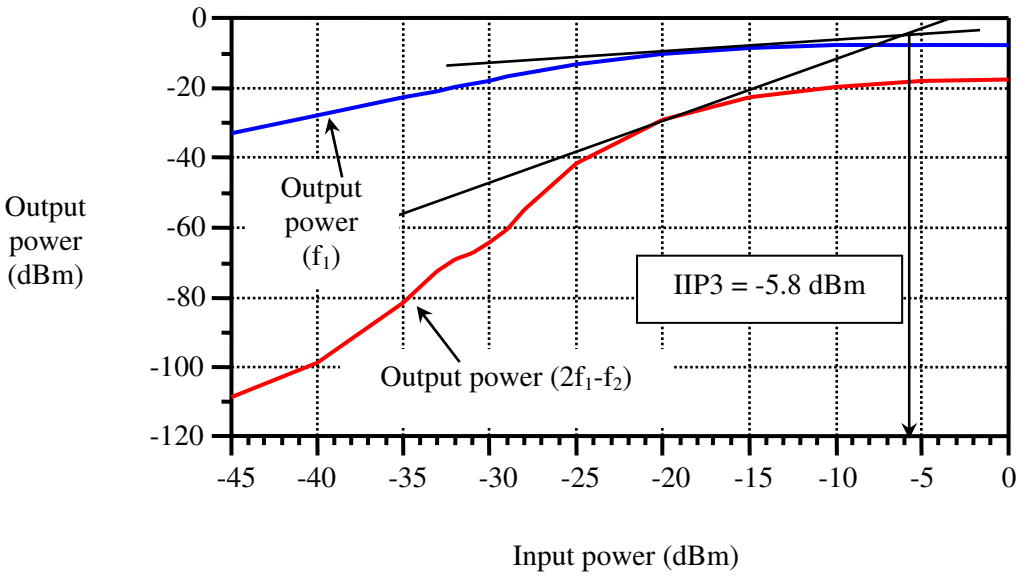


Figure 80: Simulated third-order intercept point

Isolation is another important figure of merit for mixers. Feed-through causes signal distortion, which is unacceptable in signal transceivers, and it is therefore necessary to ensure that adequate isolation is provided in the circuit. Three feed-through simulations are considered here: RF-to-LO, RF-to-IF, and LO-to-IF. RF-to-LO feed through affects the local oscillator by letting strong interferers at the input pass to the LO. RF-to-IF feed-through might create even-order distortion. LO-to-IF feed-through may desensitize stages following the mixer. RF-to-LO, RF-to-IF, and LO-to-IF feed-through simulations are presented in Figure 81. It is worth noting that the simulated isolation of better than 100 dB for LO/IF feed-through is a result of an unrealistic model for the mixer. Real circuits will be unbalanced to some extent.

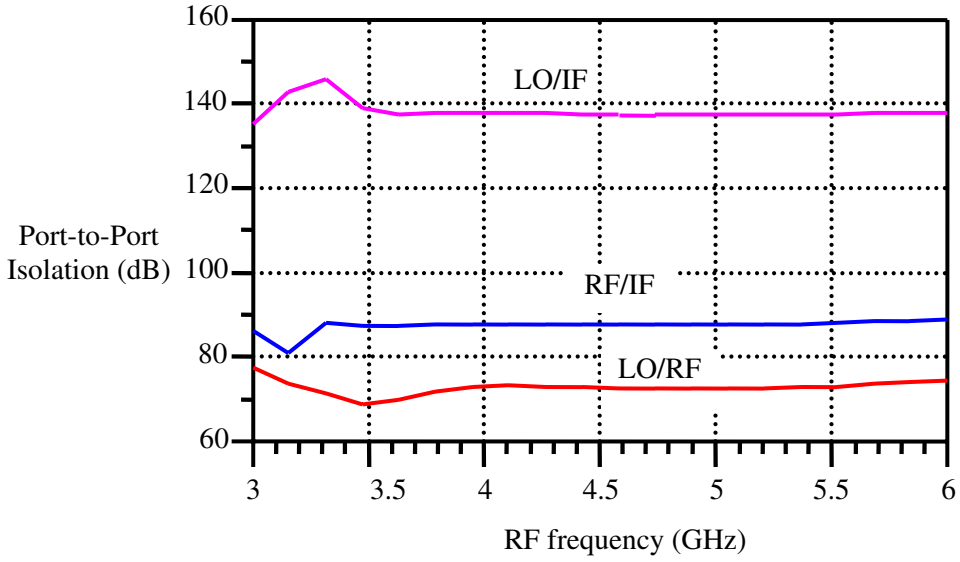


Figure 81: Simulated RF-to-IF, LO-to-IF and RF-to-LO feed through versus RF swept frequency

4.2.6 Experimental Results

The double-balanced Gilbert Cell mixer was fabricated using a 0.35 µm SiGe HBT process. A photograph of the mixer is shown in Figure 82. The chip size is 1.8 x 2 mm² including pads.

The double-balanced Gilbert Cell mixer can be operated as a down-converter or as an up-converter. As a down-converter, the mixer operates with an RF input of 4.9 GHz and a local oscillator (LO) input of 5.1 GHz. As an up-converter, the mixer operates at a RF frequency of 10.1 GHz with an applied LO frequency of 5.1 GHz.

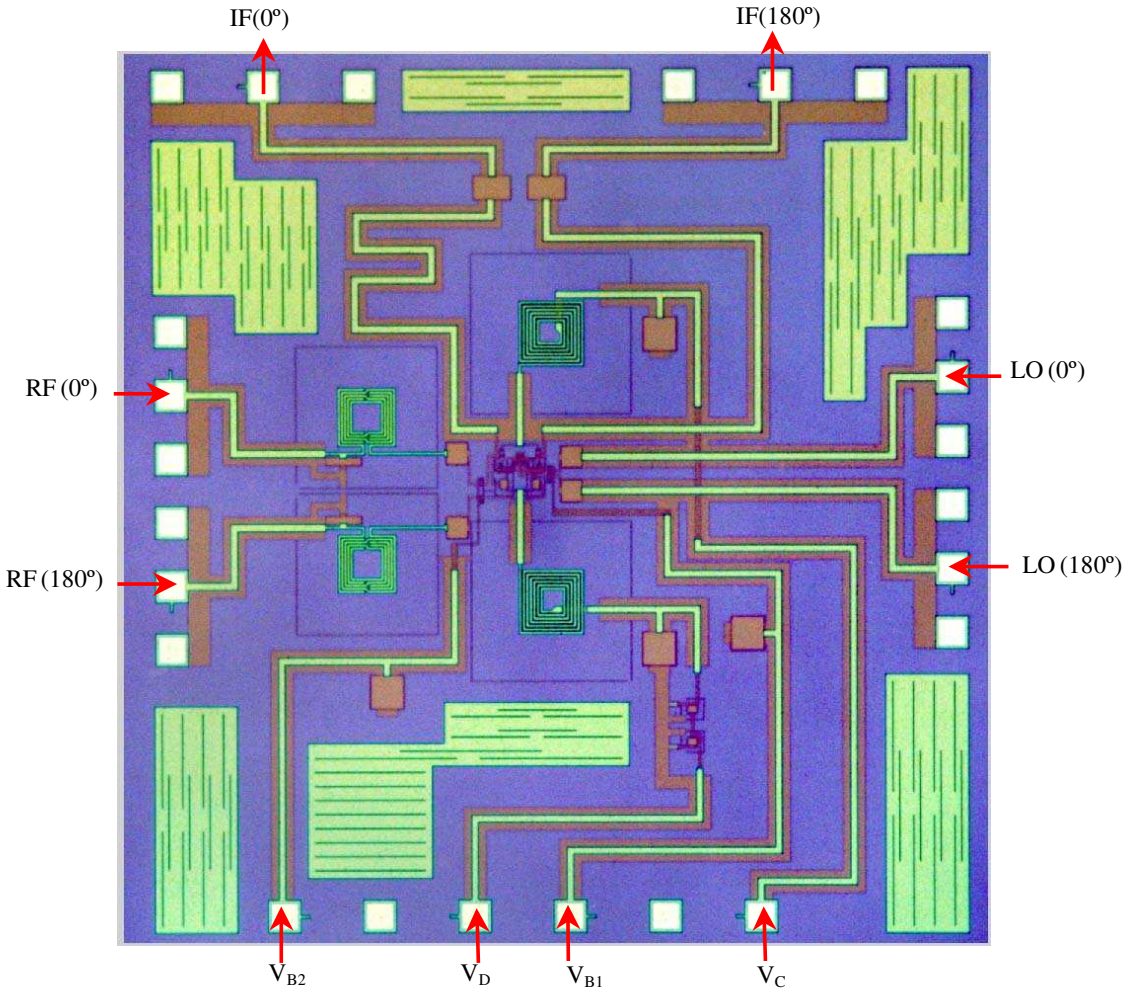


Figure 82: Die photo of the double-balanced Gilbert Cell mixer

4.2.6.1 Measurement Setup

On-wafer probe testing was carried out using 100 µm pitch dual probes in GSGGSG configuration. The setup included broadband off-the-shelf 180° hybrid couplers at the RF&LO inputs and the IF output to generate the differential input and output signals. Two controlled RF sources were used, one for the RF input and one for the LO, and a spectrum analyzer. All cable,

connector, and probe losses were measured with a network analyzer and taken into account. The measurement setup is shown in Figure 83.

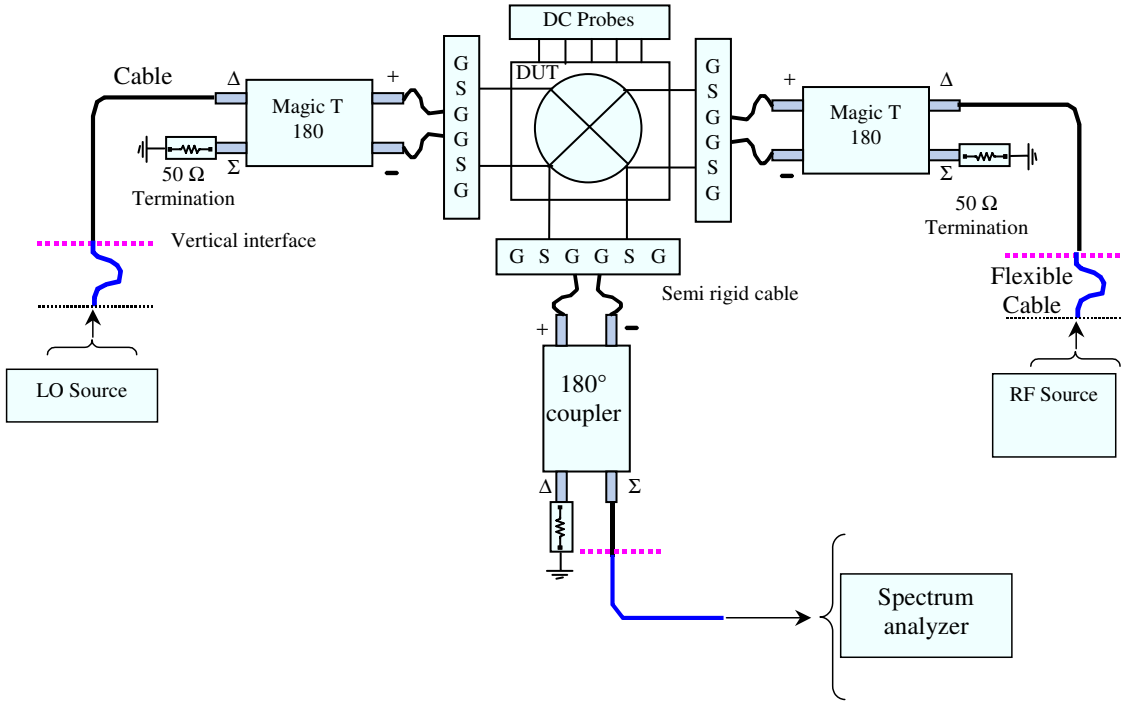


Figure 83: Measurement setup for the Gilbert Cell mixer

4.2.6.2 Measured Down-Converter Performance

The measured output spectrum of the mixer as a downconverter with a 4.9 GHz input signal and 5.1GHz LO signal is shown in Figure 84. Cable and probe losses have not been de-embedded.

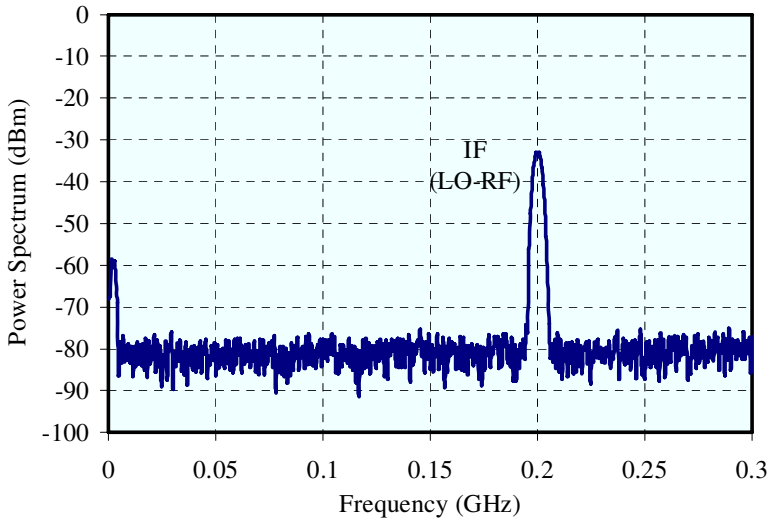


Figure 84: Measured output spectrum of the mixer operating as a downconverter

To examine the mixer's LO power requirement, the conversion gain was measured at an RF input frequency of 4.9 GHz while sweeping LO power. A peak conversion gain of 8.7 dB was achieved with 3 dBm LO power. The conversion gain profile versus LO input power is shown in Figure 85. Reducing LO power to -7 dBm resulted in a modest reduction of conversion gain to 8 dB. The measured conversion gain of 8.7 dB differs from the simulated values by about 3 dB. This can be attributed to the fact that the quality factors of the on-chip inductors are 30% lower than that used in the simulations.

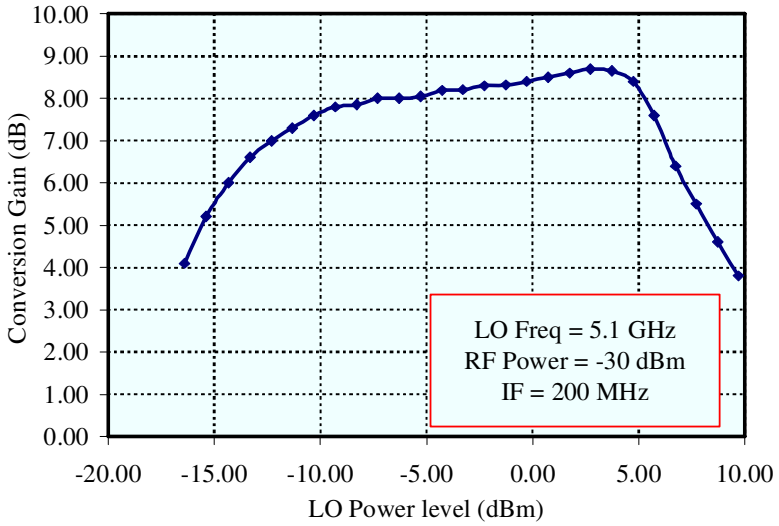


Figure 85: Measured conversion gain versus LO input power

The Gilbert Cell mixer demonstrates wideband characteristics. Measurements show that it operates normally for RF input frequencies from 4 GHz up to 5.2 GHz. Figure 86 plots the conversion gain over input RF frequency. The measured conversion gain is 8.5 ± 0.5 dB across the RF bandwidth of 4–5.2 GHz for an LO power of +2 dBm.

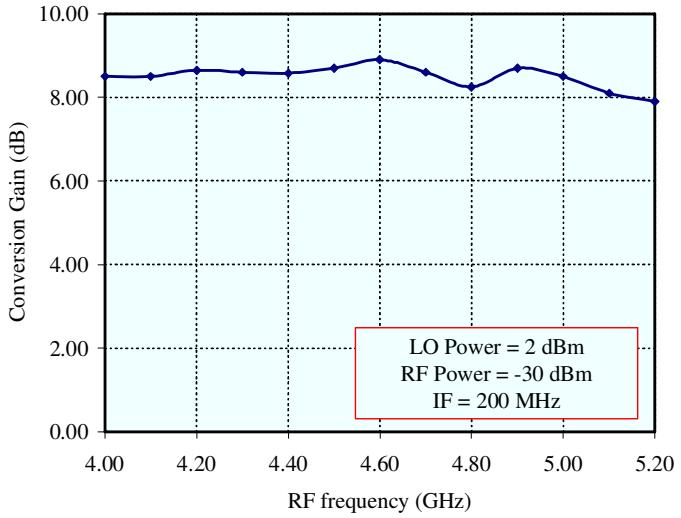


Figure 86: Measured conversion gain versus RF frequency

The measured conversion gain varies between ±1 dB when the IF is changed from 0.2 to 0.9 GHz using a swept LO. This is shown in Figure 87.

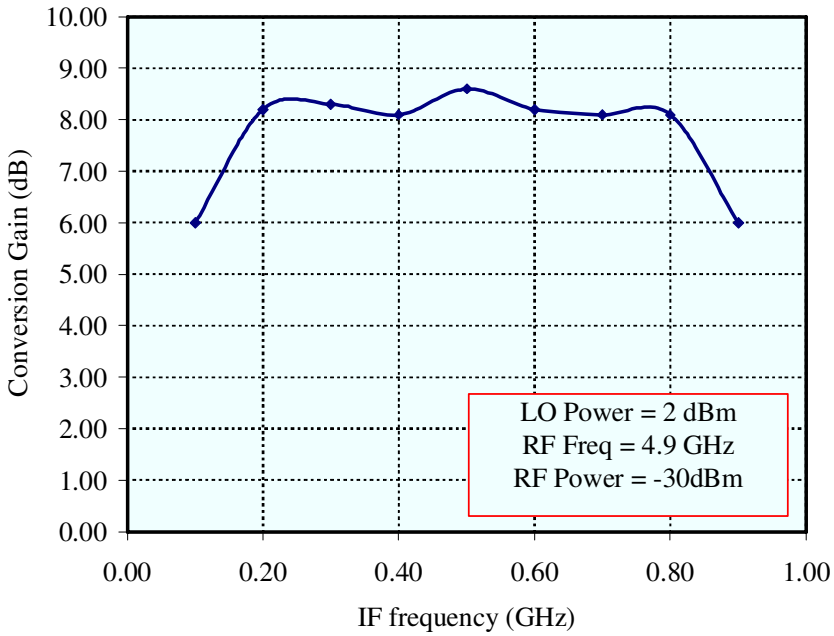


Figure 87: Measured gain conversion versus IF frequency

The measured 1-dB compression point of the conversion gain is achieved with a RF input power of -23 dBm. This is illustrated in Figure 88.

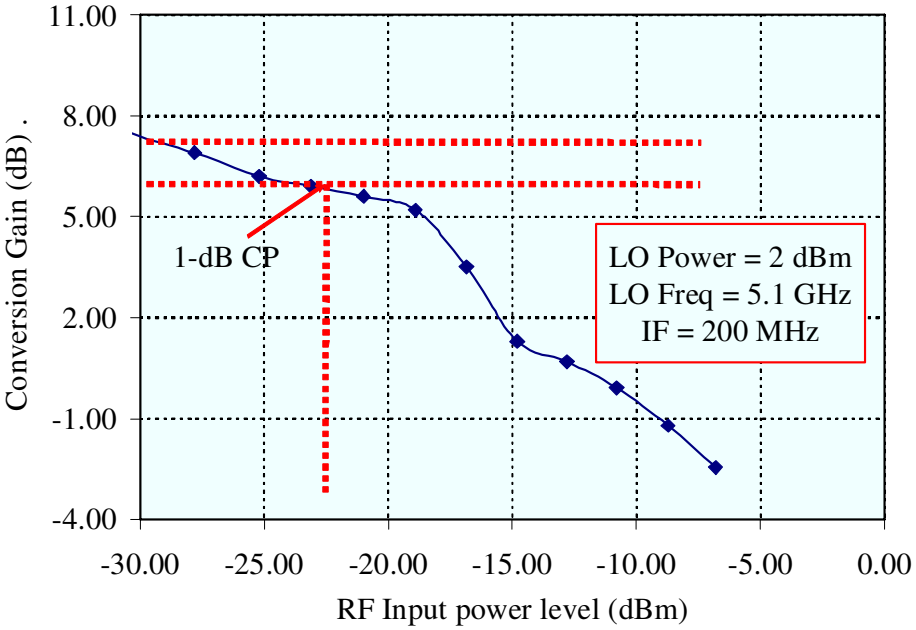


Figure 88: Measured 1-dB compression point of the Gilbert Cell mixer

The harmonic signature for the double balanced mixer is shown in Figure 89. Two tones, with equal power, were applied to the RF port at f_2=4.89 GHz and f_1=4.9 GHz with an input LO of 2 dBm at 5.1 GHz. Fundamental tones of 200 and 210 MHz and the third order products of 190 MHz and 220 MHz were observed at the IF port.

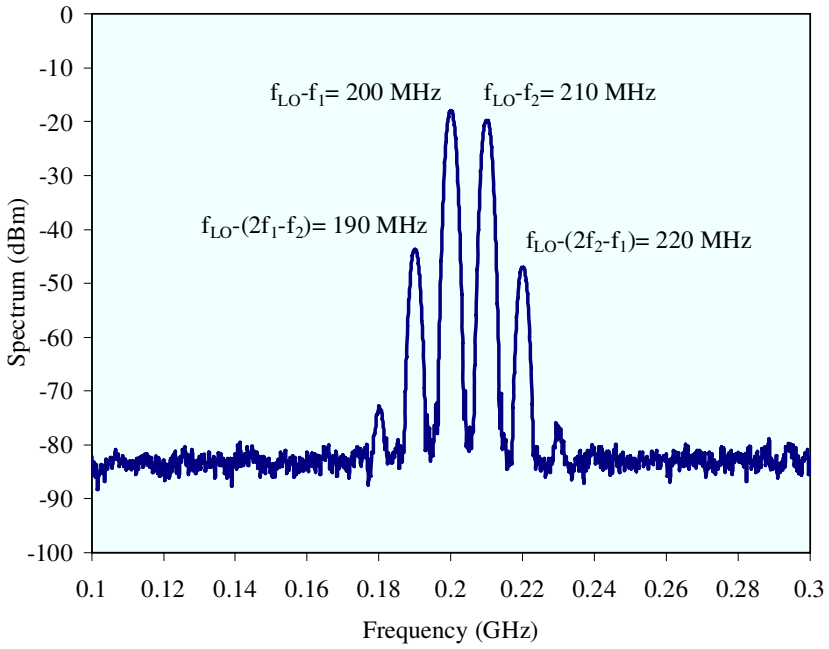


Figure 89: IF spectrum for the third-order intercept point measurement

Figure 90 shows the measured two-tone inter-modulation performance of the mixer versus RF input power at 4.9 GHz and with an LO power of 2 dBm. The IIP3 was found to be –2.5 dBm.

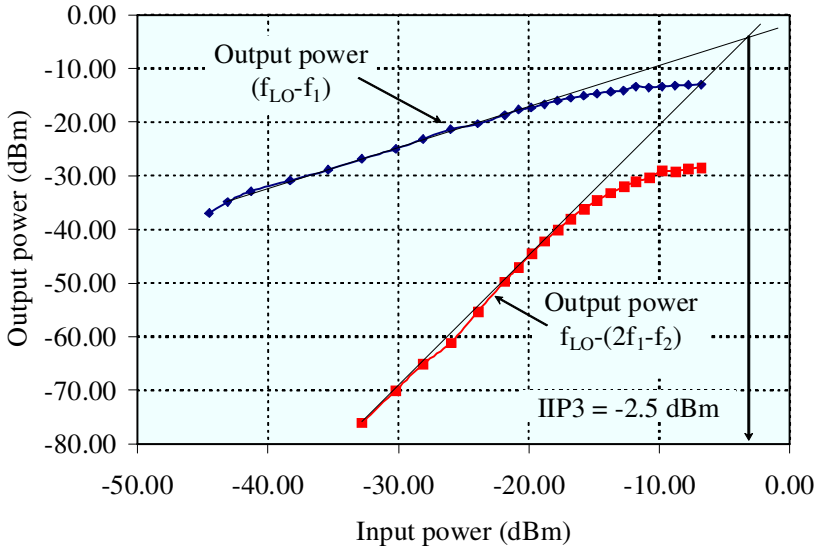


Figure 90: Fundamental and IM3 power versus RF input power

The LO-RF isolation of a down-converter is especially important since, in general, the LO frequency is close to the desired RF signal frequency and is therefore difficult to filter. Furthermore, due to intermodulation requirements, the LO power is typically an order of magnitude larger than the IF input, thereby compounding the problem. For RF frequencies below 5.2 GHz, the double-balanced down-converter has RF/LO, LO/IF and RF/IF isolation in excess of 30 dB. This is shown in Figure 91 to Figure 93.

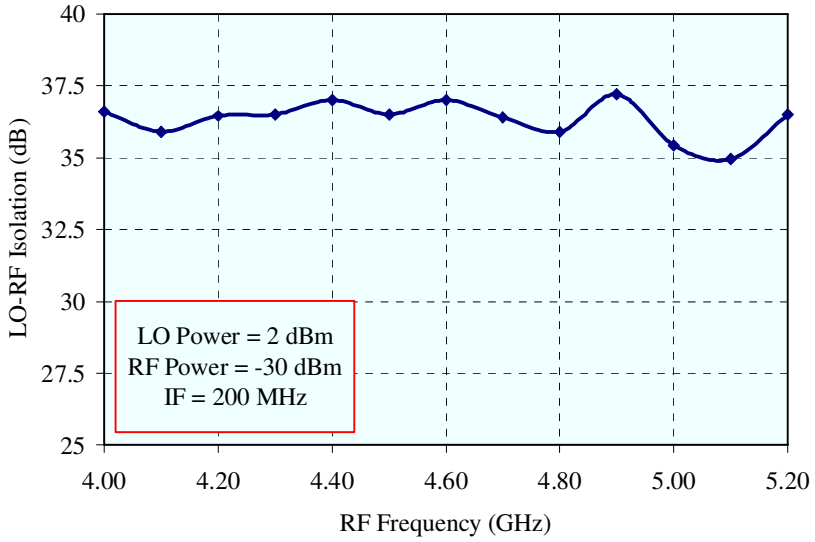


Figure 91: RF-to-LO feed through versus RF frequency

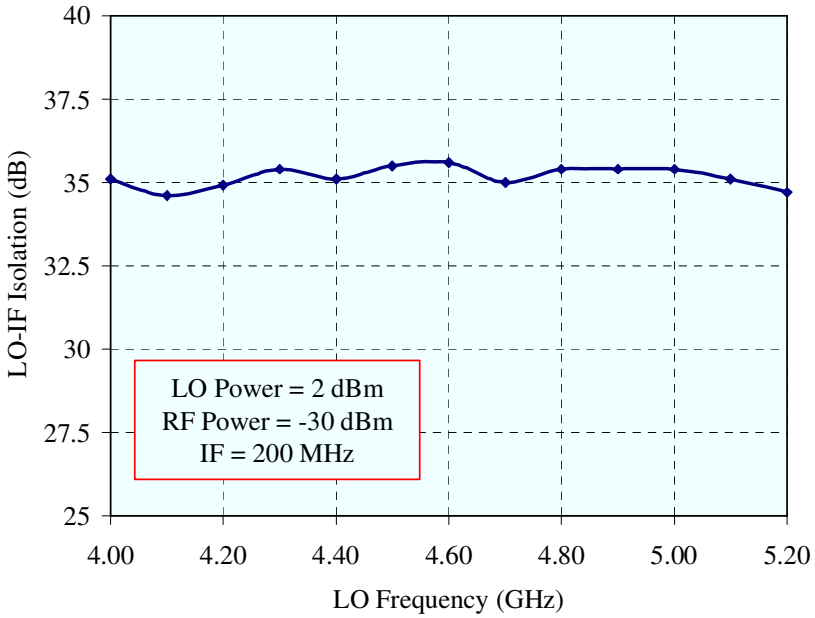


Figure 92: LO-to-IF feed through versus LO frequency

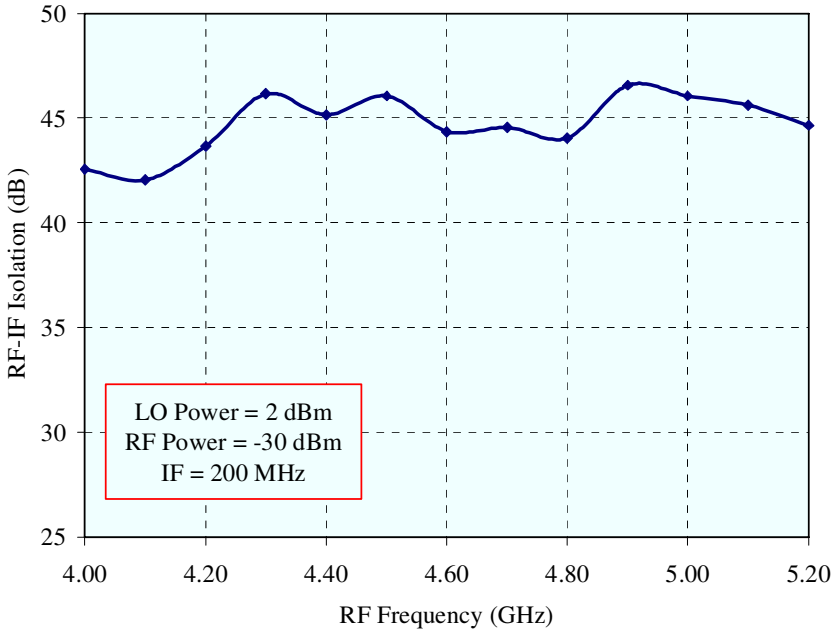


Figure 93: RF-to-IF feed through versus RF frequency

The input matching for the mixer at the RF port is shown in Figure 94. The RF input is well matched to 50Ω. The match is below –15 dB across the entire 2 GHz RF system bandwidth.

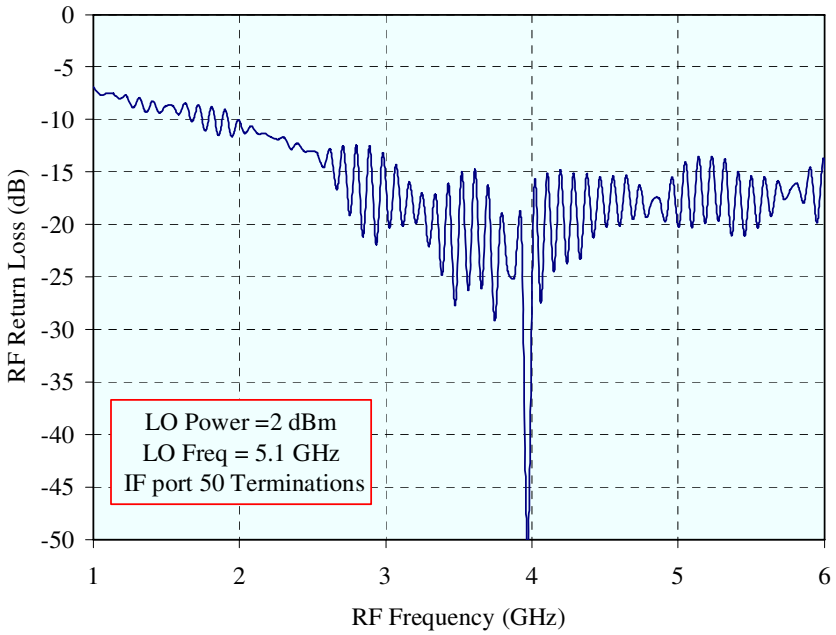


Figure 94: RF-port return loss of the Gilbert Cell mixer

Measurements of the noise figure were carried out on-wafer using an Agilent N9020A MXA Signal Analyzer. Figure 95 plots the single side band noise figure (NFSSB) as a function of the LO power at 5.1 GHz with an RF input at 4.9 GHz. It can be seen that the noise stays relatively constant when the LO input power is swept from -5 to 10 dBm. At the optimum LO power the noise figure is equal to 7.8 dB.

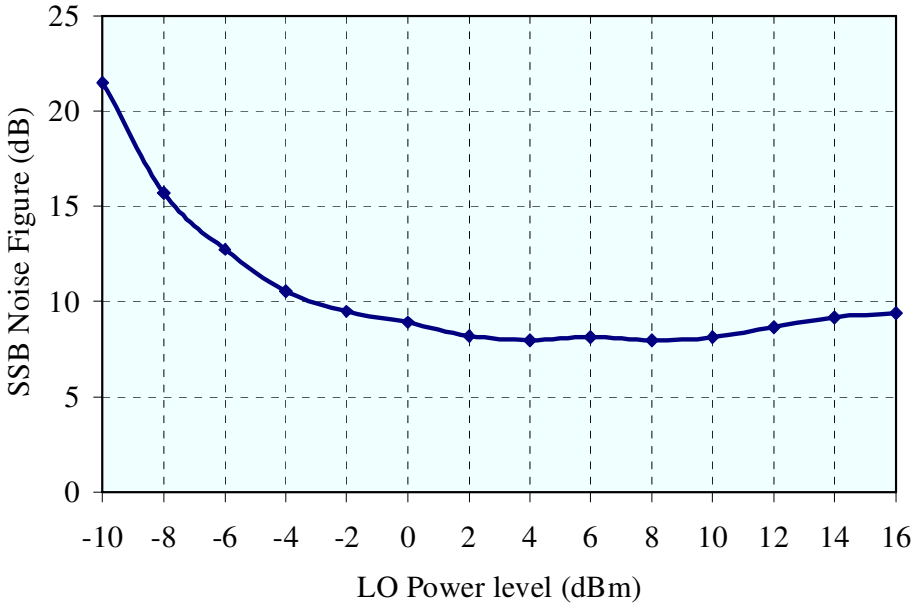


Figure 95: Noise figure versus LO input power

5 RFICs for Adaptive Phased Arrays

5.1 4-Bit Vector Modulator for Adaptive GPS Phased Arrays

5.1.1 Introduction

Variable amplitude and phase weights are required for adaptive GPS phased arrays in order to generate antenna pattern nulls in the direction of jammers. These variable weights can be achieved using a 4-bit vector modulator, the design of which is described in this section.

The 4-bit vector modulator was fabricated using a 0.35 µm silicon germanium (SiGe) heterojunction bipolar transistor (HBT) BiCMOS process. The design frequency was chosen to be 1.2 GHz (note that GPS frequencies are 1227.6 MHz & 1575.42 MHz).

The design was simulated in Agilent ADS, laid out using a combination of Mentor Graphics IC Station and Agilent ADS, and verified using Mentor Graphics Calibre. The tape-out was Dec. 2007.

5.1.2 Silicon Adaptive Phase Array Architectures

Adaptive phased arrays have been implemented recently using silicon radio frequency integrated circuits (RFICs). Although both transmit and receive arrays are possible, as shown in Figure 96, it is the receive array which is of interest for GPS phase arrays since it is capable of attenuating interferers.

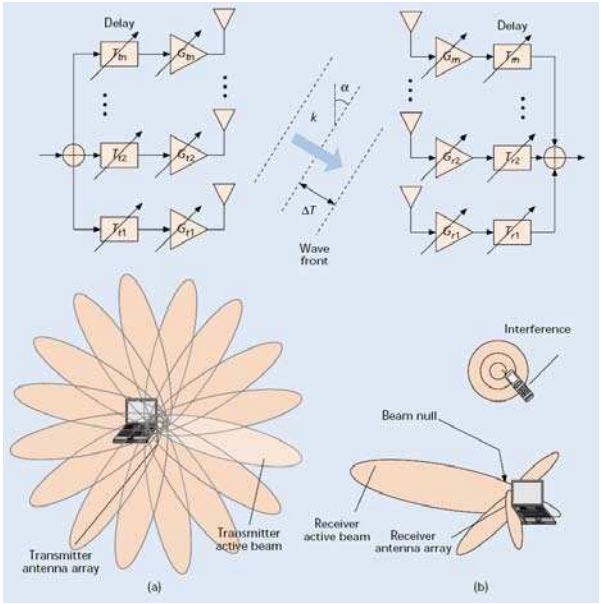


Figure 96: Phased array transmitter (a) focuses the beam at a desired angle whereas a phased array receiver (b) focuses on the desired signal while attenuating an interferer coming from another direction

Different architectures exist to implement the adaptive arrays in Figure 96, and these are shown in Figure 97 for a two-element array. For simplicity only weights with phase shifting are shown in Figure 97. There are a variety of possible locations for the phase shifter such as at the RF (a), at the IF (b), digitally in DSP (c) or in the LO path (d).

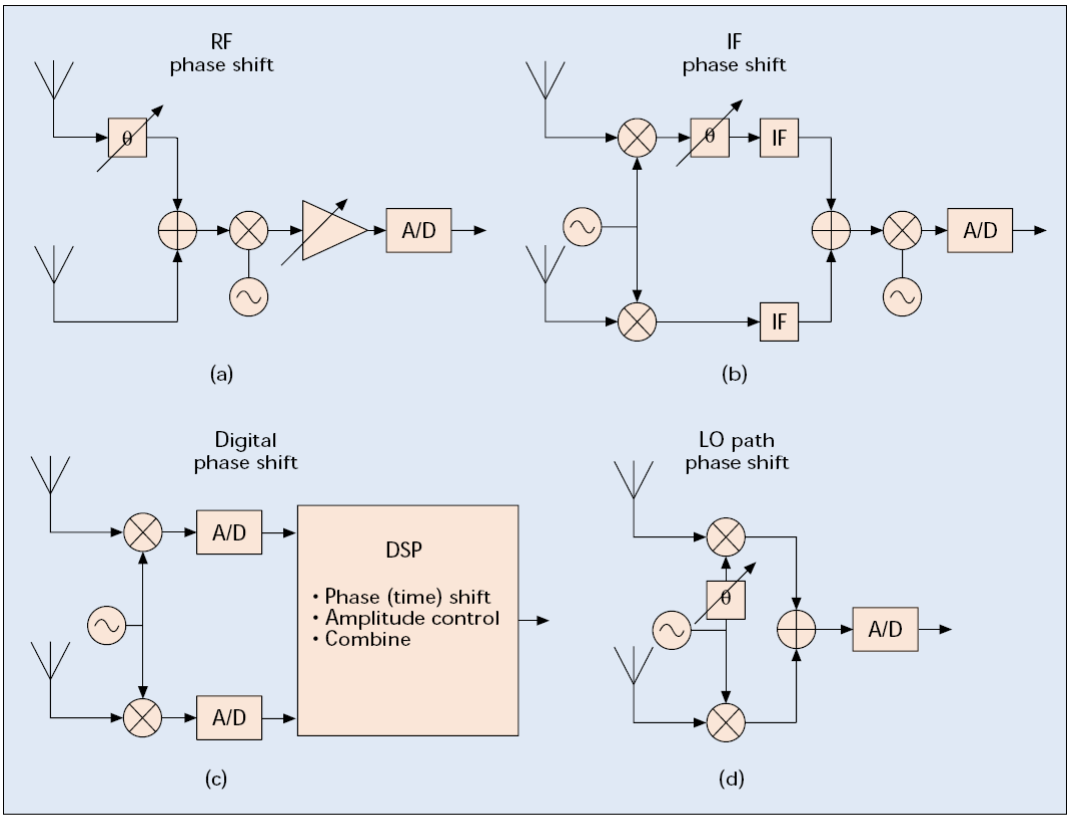


Figure 97: Different architectures for phase shifting in a two-element adaptive array receiver: (a) RF phase shifting, (b) IF phase shifting, (c) digital phase shifting and (d) LO path phase shifting

Each of these architectures has advantages and disadvantages which lead to trade-offs in power consumption, capacity, silicon area, and system reliability. Specifically:

RF phase shifting and RF signal combining

- Advantage: lower power consumption since there only needs to be one IF/baseband stage.
- Advantage: the interferers are nulled out at RF so the linearity requirements of the IF/baseband stage are reduced.
- If the signal is delayed by time, τ, the carrier at frequency f_c undergoes a phase shift equal to $2\pi f_c\tau$. Since a phase shift of θ is equivalent to a phase shift of $2\pi + \theta$, the phase shifter only needs to provide phase shifts between 0 and 2π
- But, the gain should be constant across phase shifts, and the phase shifter should have low loss.

IF phase shifting	– Disadvantage: phase shifters in the IF stage increase power consumption because in an n element receiver, there will have to be n downconversion mixers before the phase shifters. – Disadvantage: since the value and therefore the size of passive components (i.e., inductors, capacitors, and transmission lines) needed to provide phase shift is inversely proportional to the frequency, implementing the phase shifters at IF will increase system area.
Digital phase shifting	– Advantage/Disadvantage: A baseband digital delay increases the flexibility of the system; however, this advantage is offset by the high power consumption of such a system, which is essentially equivalent to n receivers operating in parallel while sharing no blocks except for the frequency synthesizer. – Disadvantage: tough performance criteria on the analog-to-digital (A/D) converter in order to provide accurate delay. – Disadvantage: the interferers are still present so the linearity and dynamic range of the IF stage and A/D converter will also have to be substantially higher leading to higher power consumption.
LO phase shifting	– Since the downconversion mixers have their best performance when they are hard-driven, the LO stages should preferably be operated in saturation. – Advantage: each path will have a constant gain irrespective of phase shift since the output of the VCO has constant amplitude, the amplitude and phase variations can be completely decoupled.

Prof. Gabriel Rebeiz compared LO/IF scanning v. RF scanning in a workshop at the International Microwave Symposium in 2007. When comparing these two architectures, shown in Figure 98 and Figure 99, he stated that "There is a reason why our 'fathers' have built the RF architecture! It offers superior performance in defense environments." For LO/IF scanned arrays there is one mixer per element which can generate a lot of intermods. LO distribution over large arrays is a problem, although there is easy power combining at the IF, which is good, but LO/IF scanning suffers from mixer linearity problems in large interferer environments. For RF scanned arrays (the more traditional architecture) no mixers are required, thus no intermods, and hence it is a linear system (which is good). RF scanning requires RF phase shifters and RF power combining which can sometimes be quite challenging but are possible on a RFIC chip. Furthermore, an RF scanned array can be made to be very linear and can handle large interferers.

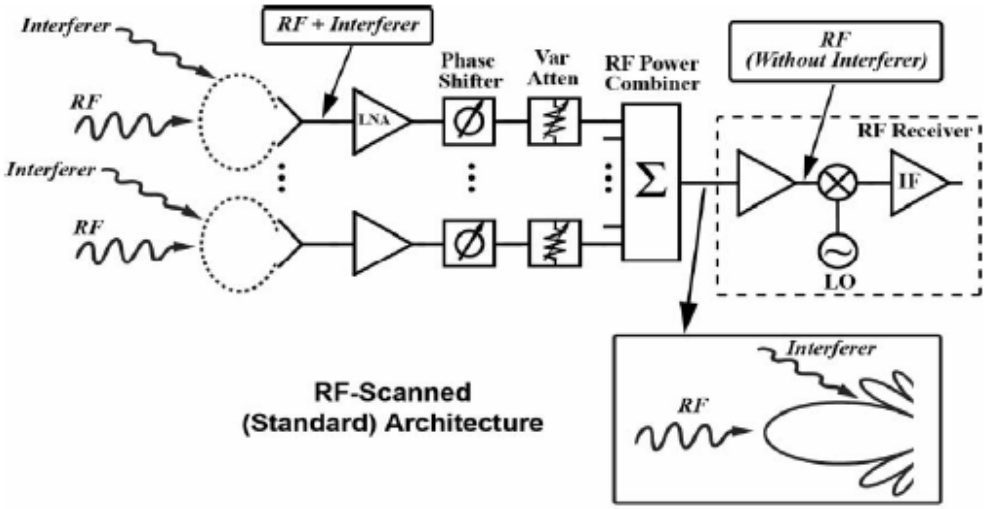


Figure 98: RF-scanned architecture for an adaptive phased array receiver

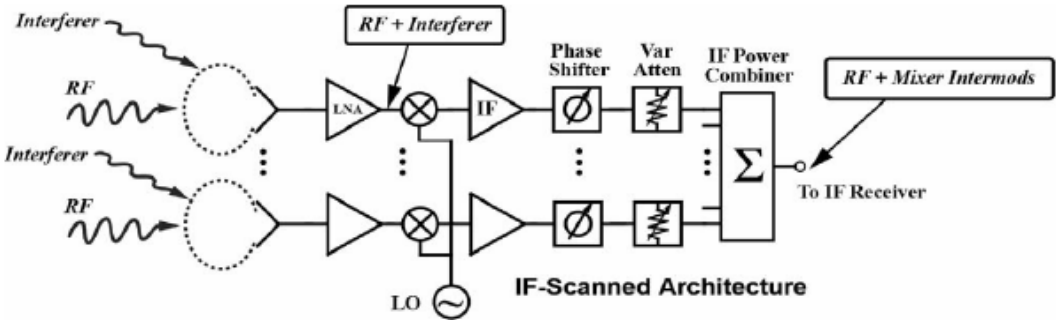


Figure 99: IF-scanned architecture for an adaptive phased array receiver

5.1.3 Topology

The topology chosen for the 4-bit vector modulator includes two 4-bit phase shifters and two Wilkinson combiners/splitters. This is shown in Figure 100**.** The two 4-bit phase shifters use the topology shown in Figure 101 although the L_r inductors are not used. This vector modulator topology functions as follows. The Wilkinson splits the input signal into 2 equal amplitude and equal phase signals that are each input to a 4-bit phase shifter. These two input signals can be considered as two in-phase, equal-amplitude vectors. The 4-bit phase shifters then phase shift each one of these vectors by a phase amount determined by the 4-bit control signal. When these phase-shifted output vectors are summed in the output Wilkinson, vector addition results in an output signal from the vector modulator that has been phase and amplitude adjusted. Since each phase shifter has 2^4=16 possible states, the vector modulator has 2^4 2^4=256 possible output states of phase/amplitude shifting with respect to the input signal.

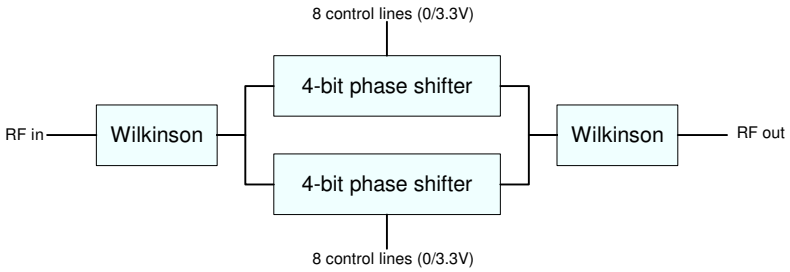


Figure 100: 4-bit vector modulator topology

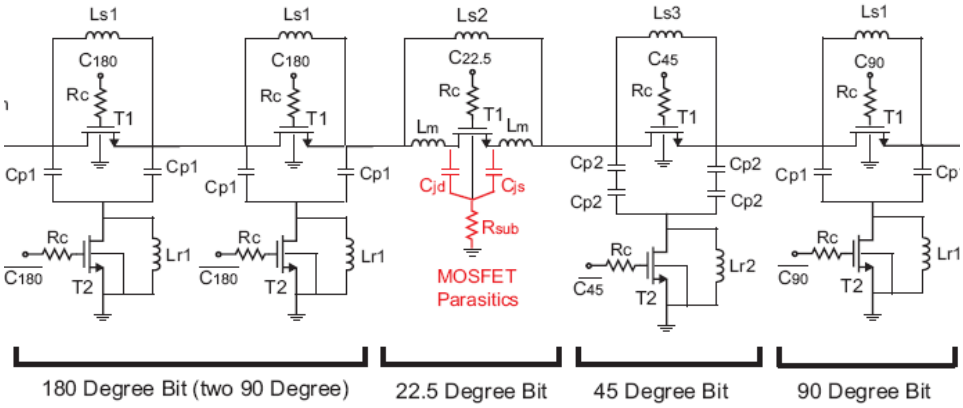


Figure 101: 4-bit phase shifter topology

For each bit in the 4-bit phase shifter of Figure 101 two CMOS devices, T1 and T2, control the signal path between the phase shift path and the reference path. Specifically, when T1 is off and T2 is on then the signal passes though a low pass filter (LPF) whereas when T1 is on and T2 is off the LPF is shorted. This short is the reference path and has a finite phase shift. The LPF is a π-network designed to have a 50 Ω characteristic impedance and a specific phase shift so that the phase difference between the π-network and the reference path is equal to the desired phase shift for the bit. The advantage of this phase shifter topology compared to a low-pass/high-pass phase shifter is low power consumption and small size; however, it has a narrower bandwidth compared to that of a low-pass/high-pass topology.

In the 4-bit phase shifter, each CMOS device is used as a variable resistance to form a simple switch since their drain-source resistance is voltage-variable in the region of V_{ds}=0 V. Thus, the drain and source voltages are set to 0 V dc, the gate is the control voltage, and the RF path is from the drain to the source. This configuration is compact and consumes very little dc power. When V_{gs}=3.3 V the FET is on while for V_{gs}=0 V the FET is off. The equivalent circuit, shown in Figure 102, is a variable resistance and capacitance, the values of which are process and device size dependent. Extra isolation between the signal and control lines is provided by R_g (which can be several kΩ because the gate current is small) but the equivalent capacitance can limit the isolation in the off-state, especially as frequency increases and its impedance lowers. Sometimes this capacitance is resonated with a shunt inductor to remove this lower impedance (although this is a narrowband solution) and then rely solely on the resistance for off-state isolation. These

inductors are shown in Figure 101 (noted by L_r), however, they are not used in the 4-bit vector modulator.

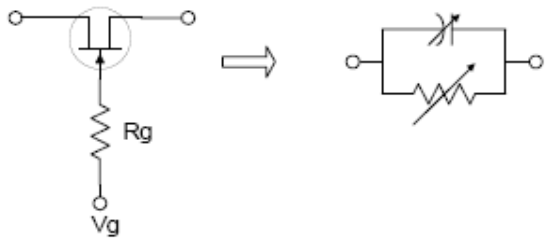


Figure 102: Equivalent circuit of the CMOS transistors used in the 4-bit phase shifter

In addition to the 4-bit phase shifter, the other component of the 4-bit vector modulator is the Wilkinson combiner/splitter. A standard lumped element version is used, a schematic of which is shown in Figure 103.

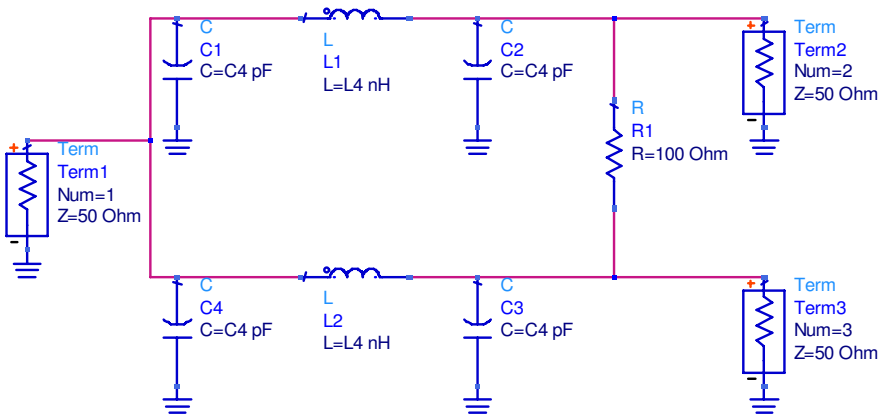


Figure 103: Lumped element Wilkinson combiner/splitter

5.1.4 Wilkinson Design

The lumped element Wilkinson, shown in Figure 103, includes two identical low-pass, π-networks. The element values for an ideal low-pass, π-network with characteristic impedance Z_o and phase change φ, at frequency ω, are shown in Figure 104. At 1.2 GHz, these elements are L_4=9.377 nH and C_4=1.876 pF.

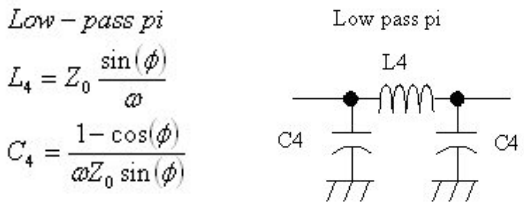


Figure 104: An ideal low-pass π -network

With no loss in the inductor these ideal elements form a perfect Wilkinson. There is, however, about 8.3 Ω of series resistance in a 9 nH realizable differential inductor. When this series resistance is introduced to the ideal Wilkinson, the performance degrades. The optimizer in Agilent ADS was used to vary L_4 and C_4, along with the 100 Ω resistance, to attempt to achieve S_{11}, S_{22}, S_{33}, S_{23} of at least -20 dB around 1.2 GHz. This optimization resulted in L_4= 9.39 nH, C_4=1.648 pF and R=108 Ω. The simulated S-parameters of the Wilkinson with the optimized L_4, C_4 and R, along with the 8.3 Ω of series resistance are shown in Figure 105.

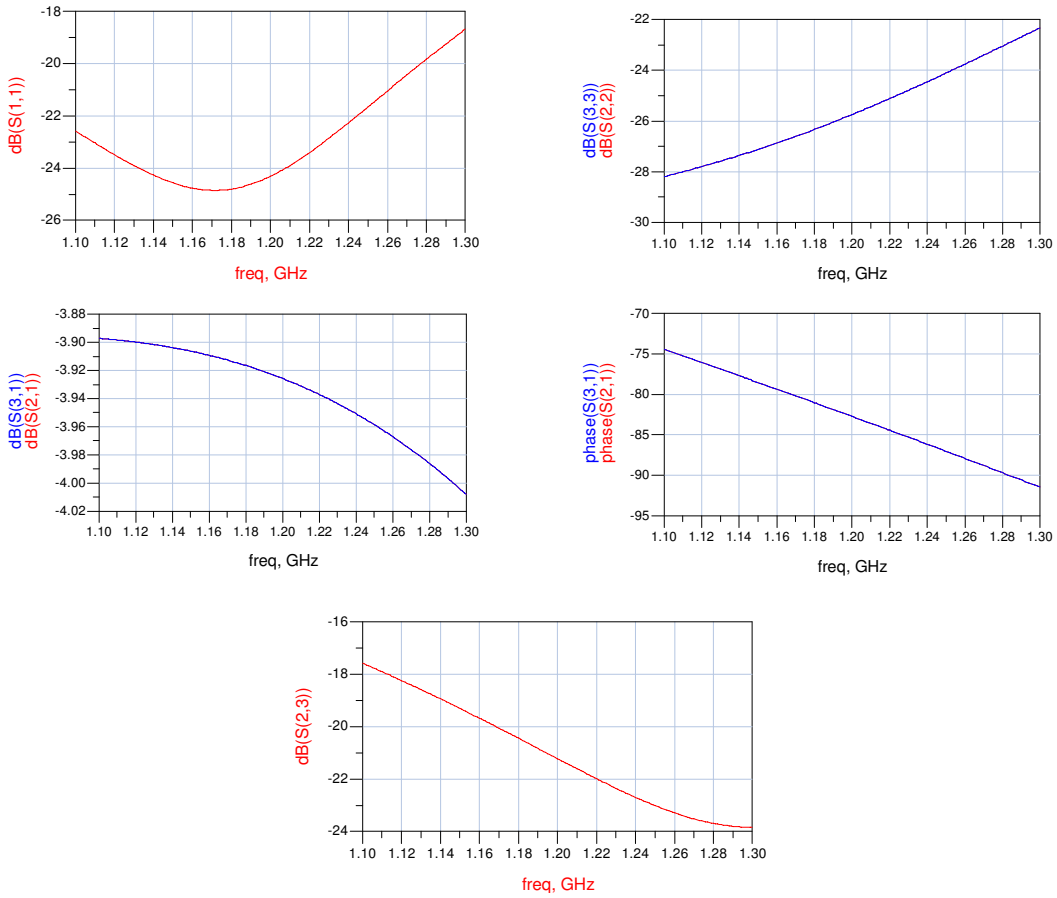


Figure 105: Simulated s-parameters of the Wilkinson combiner/splitter with optimized ideal elements

After the optimization, the optimized ideal lumped elements are replaced with physically realizable equivalent elements having foundry models. Specifically, the realizable equivalent inductor has dimensions x=y=335 µm, conductor width w=9 µm, conductor spacing s=3 µm and number of turns n=4 which gives 9.340 nH and a series resistance of 8.5 Ω at 1.2 GHz. The realizable equivalent capacitors are 40×40 µm, and the realizable equivalent resistor is a 5 µm ×4 µm low value unsalcided poly resistor.

The simulated results, Agilent ADS, of the Wilkinson with realizable elements are shown in Figure 106.

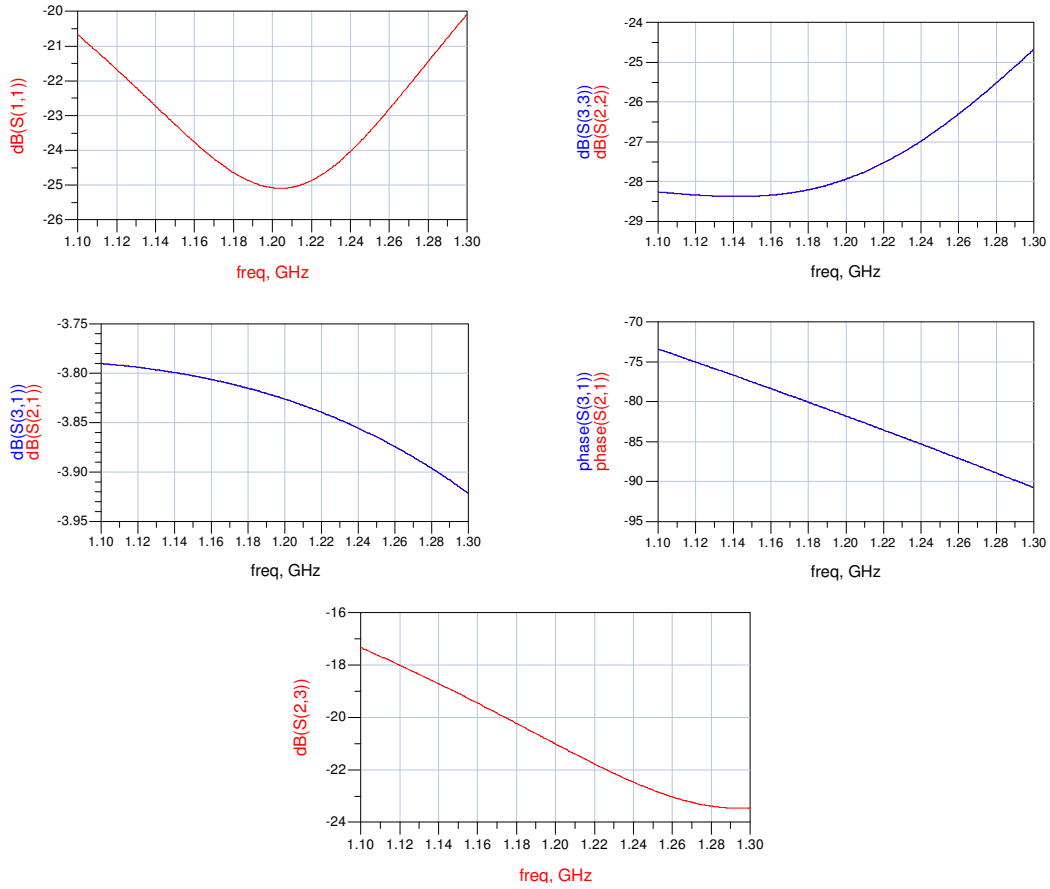


Figure 106: Simulated results for the Wilkinson with realizable elements

5.1.5 CMOS Device Sizing

Each bit of the phase shifters require both a series and a shunt CMOS device, both which need to be sized appropriately. A large device has a small series resistance, leading to a better short circuit in the on-state (which is desirable), but a large device also has a large capacitance in the off-state which degrades the open circuit on the off-state (which is not desirable) and thus the appropriate device size is a trade-off between these two extremes. Therefore available device sizes are swept by fixing emitter length and width and then sweeping the number of fingers, n, to vary the device size from the smallest to the largest. Simulations of the impedance of a single device, in both series (Figure 107) and shunt (Figure 108), confirm that larger is better for the on-state but smaller is better for the off-state. Note that with V_{ds}=0, the on-state is V_{gs}=3.3V and the off-state is 0V.

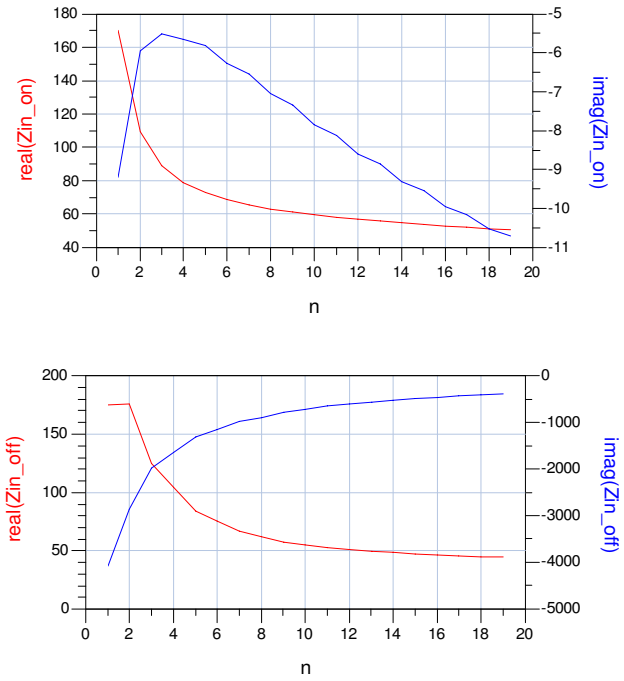


Figure 107: Impedance (Ω) of a single series CMOS device v. device size for the on and off-state

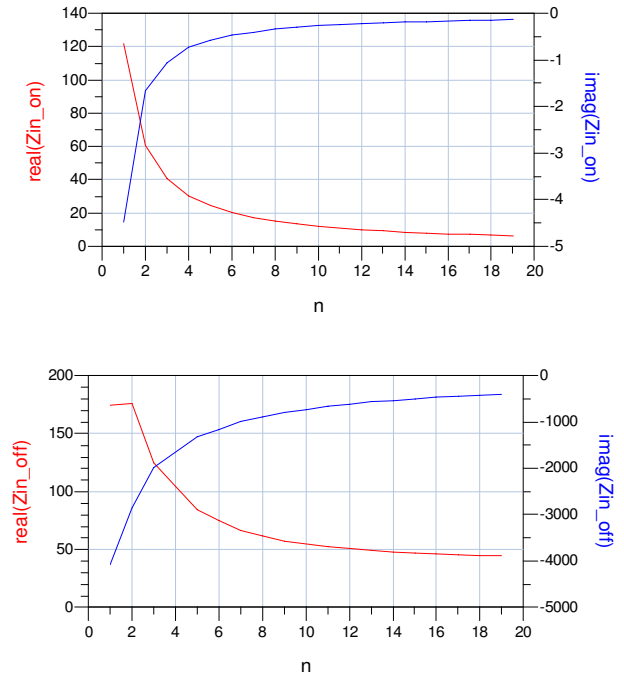


Figure 108: Impedance (Ω) of a single shunt CMOS device v. device size for the on and off-state

The simulations shown in Figure 107 and Figure 108 are somewhat useful – they show that the device probably has to be at least mid-sized for a low on resistance. It is, however, difficult to choose a device size based on impedance because it is difficult to know how low the on impedance needs to be or how high the off impedance needs to be. Therefore, a series CMOS device was simulated to give an idea of the lowest possible insertion loss (IL) and return loss (RL) for the reference (thru) state of the bit. These simulations, shown in Figure 109, show that for the on-state (left) it seems like the best RL is 20 dB and the best IL is 0.9 dB. Isolation in the off-state (right) is at least -30 dB. Also, the on-state phase shift is between 2º and 6º. These results show the performance limit of the reference or thru state.

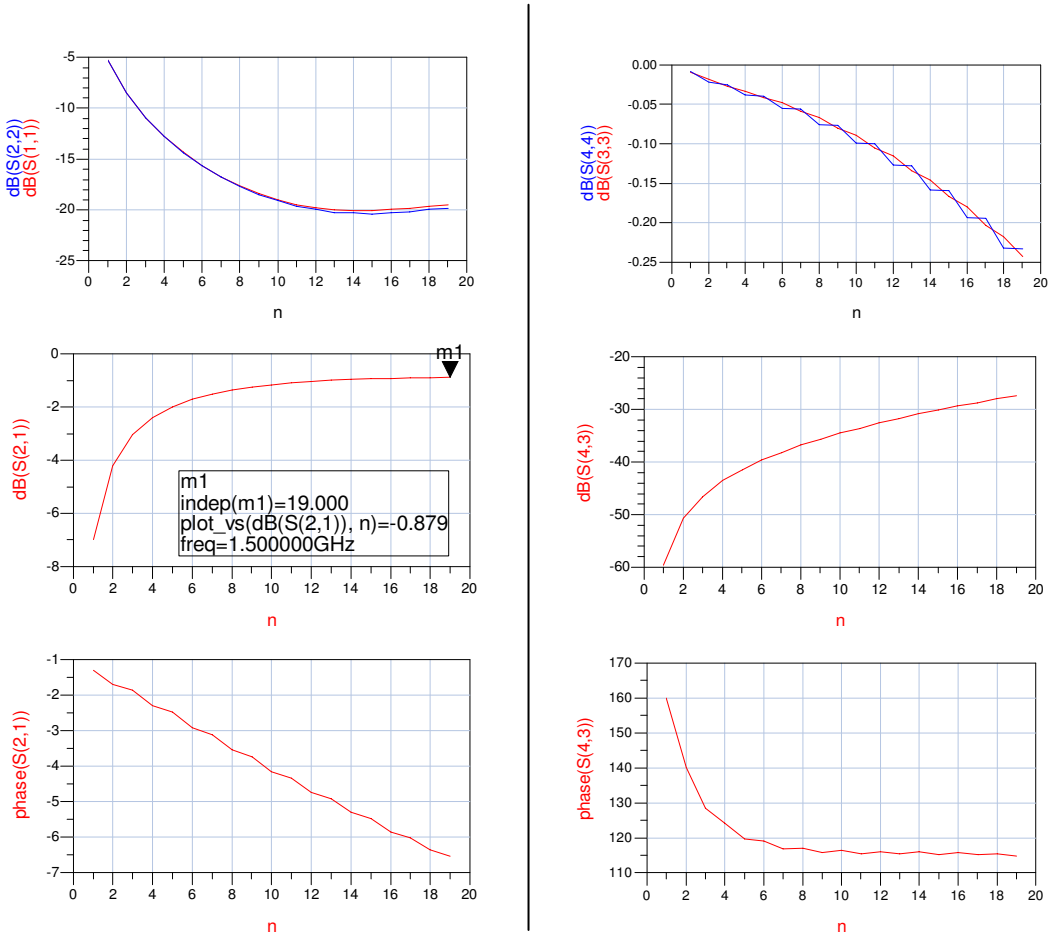


Figure 109: Simulated return loss, insertion loss and phase shift of a series CMOS device v. device size for the on-state (left) and the off-state (right)

The performance limit shown in Figure 109 is still optimistic, however, because when the series CMOS device is included in an actual phase shifter bit it is in parallel with a realizable lumped element. This causes the performance to degrade further and also changes the phase shift. For example, for a 95º bit with realizable inductors and capacitors (with perfect open circuits connected to the shunt capacitors instead of off-state CMOS devices), the RL drops to 18 dB (at a new optimum device size), IL increases to at least 1.1 dB, and the phase shift increases to 11º. These simulated results are given in Figure 110.

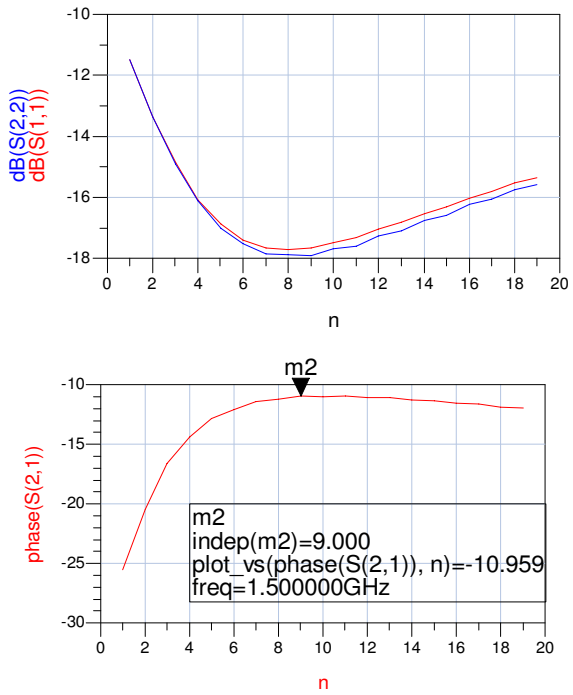


Figure 110: Reference state of a 95º bit v. CMOS device size

Therefore, considering the results from Figure 107 to Figure 110, the device size must be chosen by sweeping it within a particular bit. Nevertheless, the simulated results of devices alone (Figure 107 to Figure 110) are useful because they provide an approximation of the performance that may be expected. For example, in each bit the phase shift path should be designed using a low-pass π-network with θ+10º since the reference path is likely to have a phase shift of around 10º, then the device size may be swept for optimal performance. After selecting the device size then the π-network can be adjusted since the reference phase shift is likely not going to be exactly 10º.

5.1.6 Phase Shifter Bit Design

A π-network for each bit was designed initially without CMOS devices by using the formulae given in Section 5.1.4. With the assumption that the reference state has a -10º phase shift as described in the previous section, the bits were designed to have phase shifts of -100º, -55º, -32.5º for phase differences of 90º, 45º, 22.5º (and 180º using two 90º bits) between the reference (thru) path and the phase shift path (π-network). This resulted in the following lumped element values for the π-networks at 1.2 GHz:

for 100º (90º and 180º bit) → L_4= 6.531 nH, C_4= 3.161 pF

for 55º (45º bit) → L_4= 5.432 nH, C_4= 1.381 pF

for 32.5º (22.5º bit) → L_4= 3.563 nH, C_4= 0.773 pF

The simulated performance of each of these π-networks, with ideal elements, is shown in Figure 111.

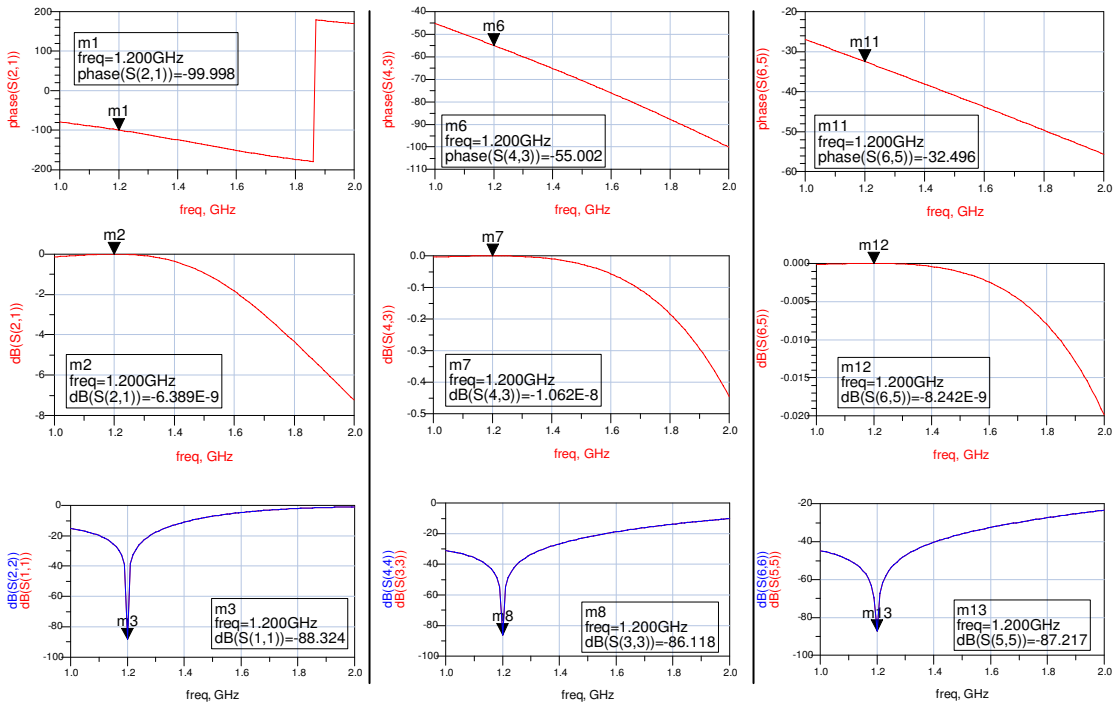


Figure 111: Simulations of the π-networks, with ideal elements, for 90º (left), 45º (centre), and 22.5º (right)

The ideal inductors are then replaced with realizable differential inductors. Differential inductors were chosen because, in the final phase shifter layout, differential inductors have shorter interconnecting lines which in turn have less impact on the phase shift of the bit.

The realizable inductors need to be selected with low series resistance while also having a high self-resonant frequency (SRF) despite these being conflicting requirements. For example, if a bit is to have a return loss less than 20 dB and an insertion loss of less than 1 dB, then the inductor must have series resistance less than 5, 9 and 10 Ω, respectively for the 90º, 45º and 22.5º bits. Obtaining these series resistances may result in a lower than desirable self-resonant frequency and thus a more variable inductance value. In the case of the 90º bit, a variation from 6.4 nH to 6.6 nH corresponds to a ±1.5º phase shift.

The chosen differential inductors, for each bit, are:

For 100º (90º and 180º bit) → the ideal value was L_4= 6.531 nH so a 6.520 nH inductor with simulated series resistance of 4.3 Ω was selected.

For 55º (45º bit) → the ideal value was L_4= 5.432 nH so a 5.422 nH inductor with a simulated series resistance of 3.7 Ω was selected.

For 32.5º (22.5º bit) → the ideal value was L_4= 3.563 nH so a 3.554 nH inductor with a simulated series resistance of 2.4 Ω was selected.

The simulated performance of the π-network for each bit, with the differential inductors and also realizable capacitor models instead of ideal capacitors, is shown in Figure 112.

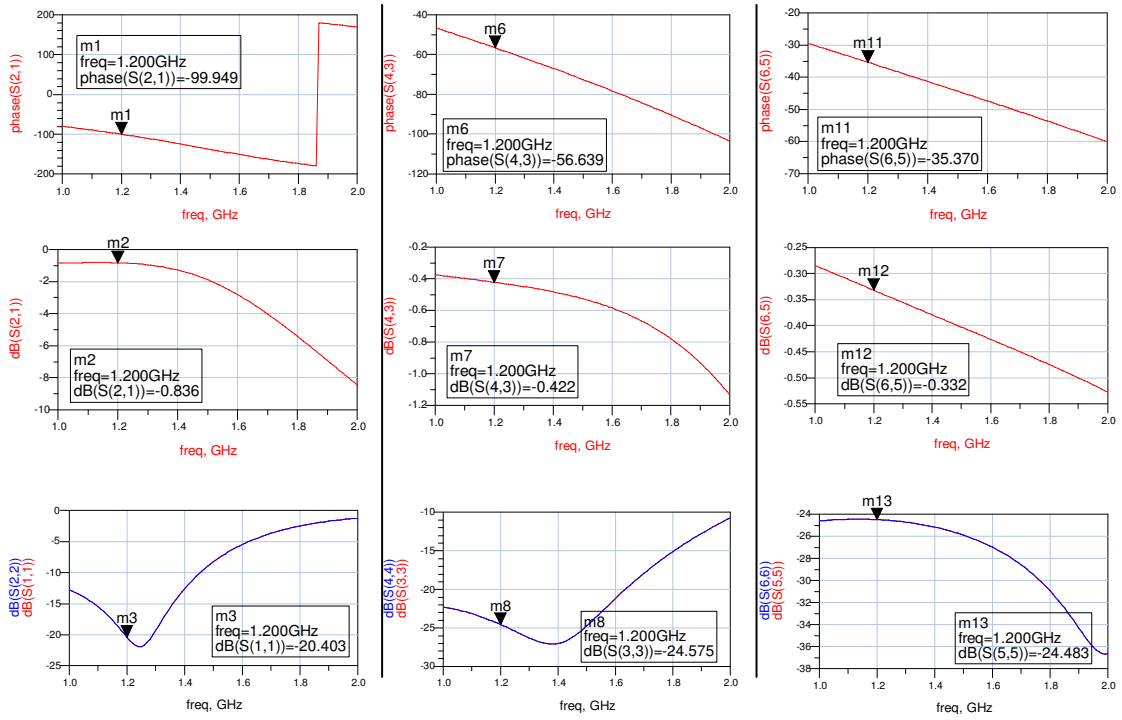


Figure 112: Simulations of the π-networks, with foundry models, for 90º (left), 45º (centre), and 22.5º (right)

Using the π-networks of realizable elements, albeit with 50 Ω terminations, the CMOS devices can be added and their sizes swept to get a better estimate of the performance of each bit (although the performance of the bits will be different in the cascaded phase shifter since the terminations for each are no longer 50 Ω, and hence both the size and lumped element values will need to be adjusted). At this stage however, the device sizes are swept for each bit alone and the sizes are chosen so that the insertion loss for the bit is as low as possible but also approximately the same for both the on and off states. The latter requirement is important so that amplitude variation between the states is minimized and hence there is an even distribution of weights. If possible, the size is also selected to minimize the input/output return loss of each bit, but this is less important than the insertion loss since the overall input/output return loss of the phase shifter can be compensated by low noise amplifiers. Finally, the ideal gate resistors are replaced by models for physically realizable 5 kΩ resistors. Simulations of each bit alone, shown in Figure 113 to Figure 117, result in the following series (n) and shunt (n_s) device sizes:

- For the 90º bit, choose n=5 and n_s= 18 (86.8º, RL = -15/-25 dB, IL = -2.1dB)
- For the 45º bit, choose n=13 and n_s=16 (49.1º, RL = -17/-24 dB, IL = -1.02 dB)
- For the 22.5º bit, choose n=17 and n_s=6 (28º, RL = -17/-19 dB, IL = -0.95 dB)
- For the 180º bit, choose n=5 and n_s=18 (172º, RL = -11/-31 dB, IL = -4.2 dB)

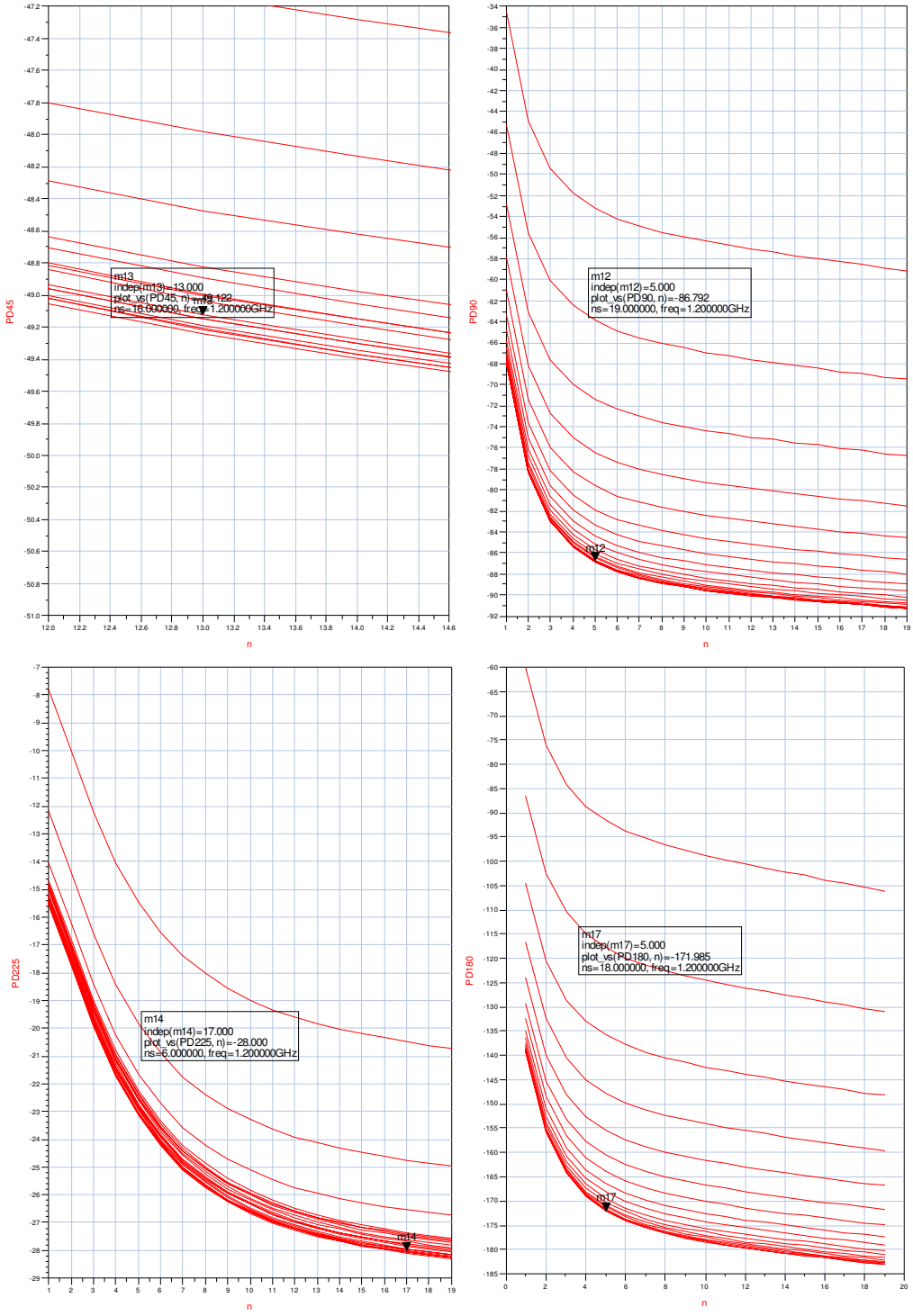


Figure 113: Bit phase shift (degrees) v. device size (series device number of fingers, n, and shunt device number of fingers, n_s) for the 45º bit (top left), the 90º bit (top right), the 22.5º bit (bottom left) and the 180º bit (bottom right)

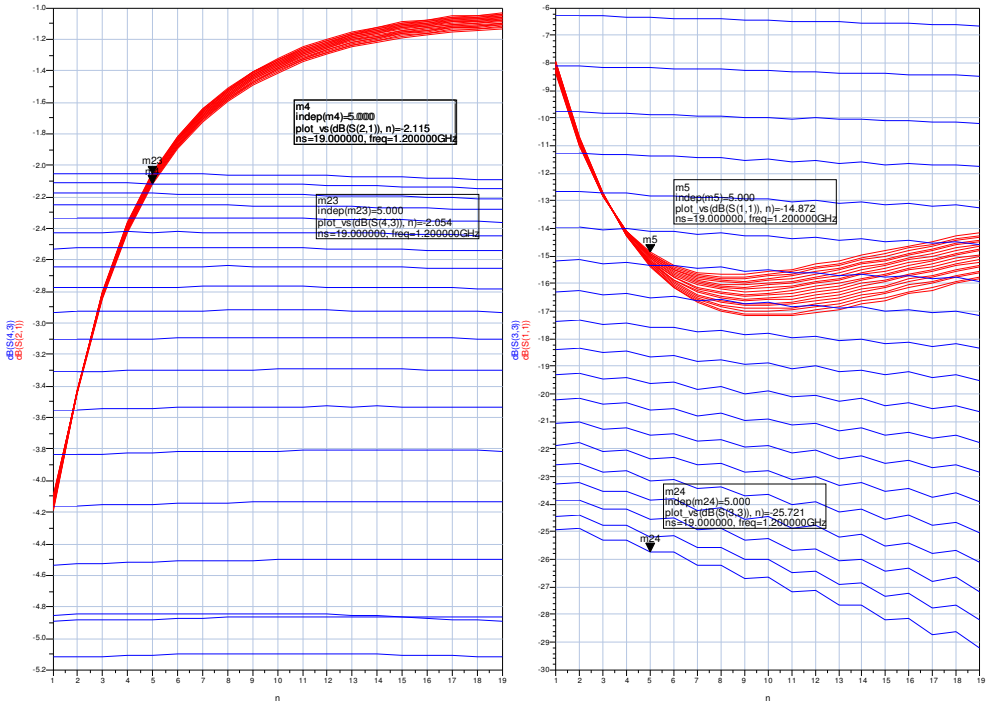


Figure 114: 90º bit insertion loss (left) & return loss (right) v. device size (number of fingers) for the reference state (red) and the phase shift state (blue)

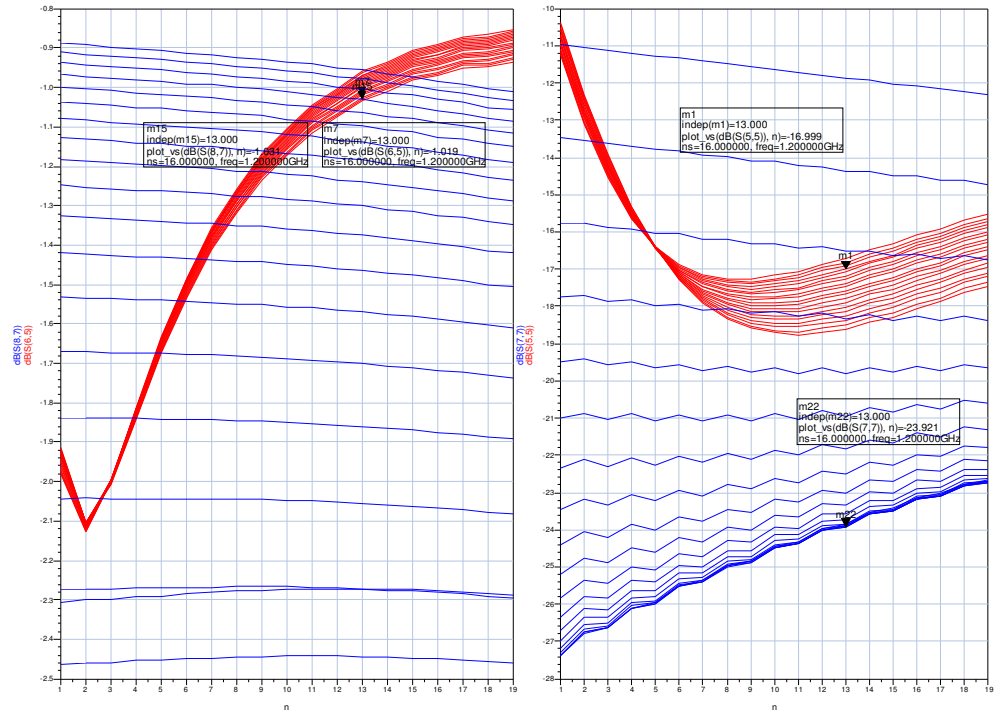


Figure 115: 45º bit insertion loss (left) & return loss (right) v. device size (number of fingers) for the reference state (red) and the phase shift state (blue)

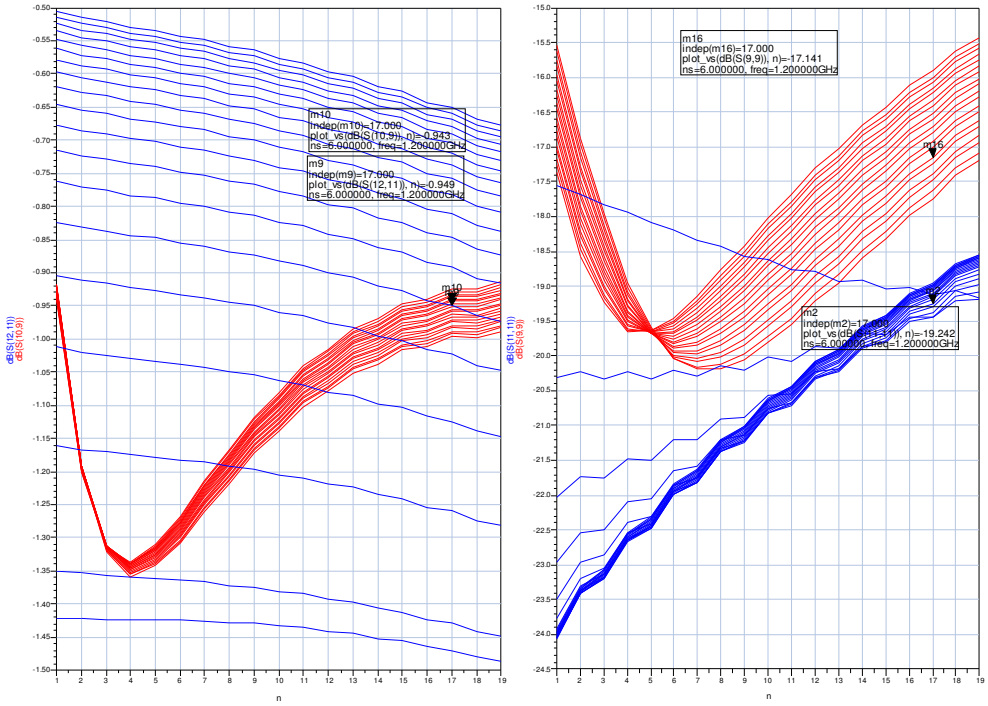


Figure 116: 22.5º bit insertion loss (left) & return loss (right) v. device size (number of fingers) for the reference state (red) and the phase shift state (blue)

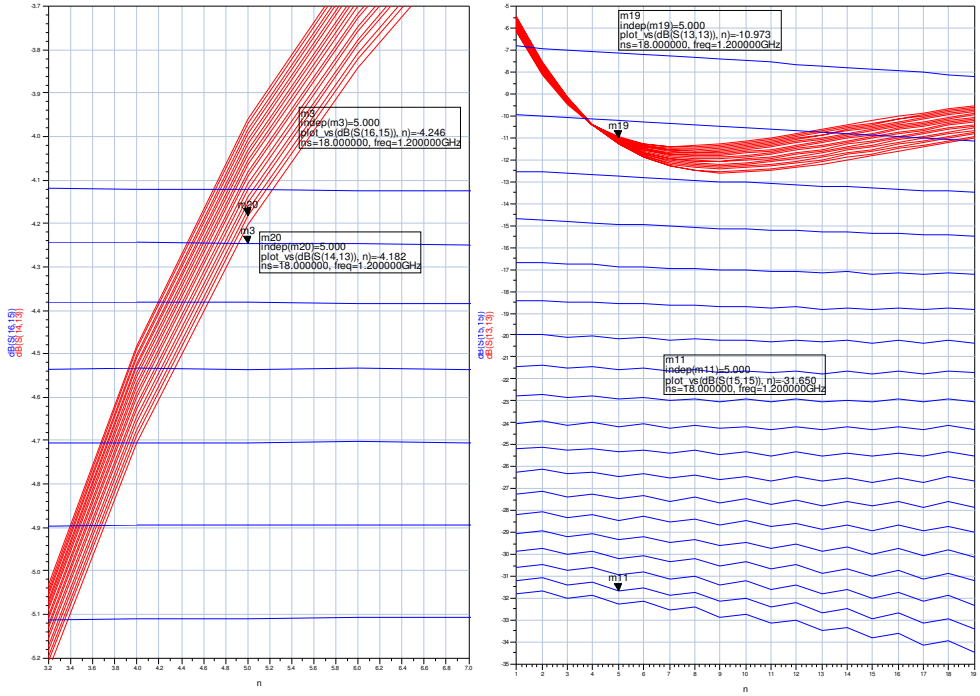


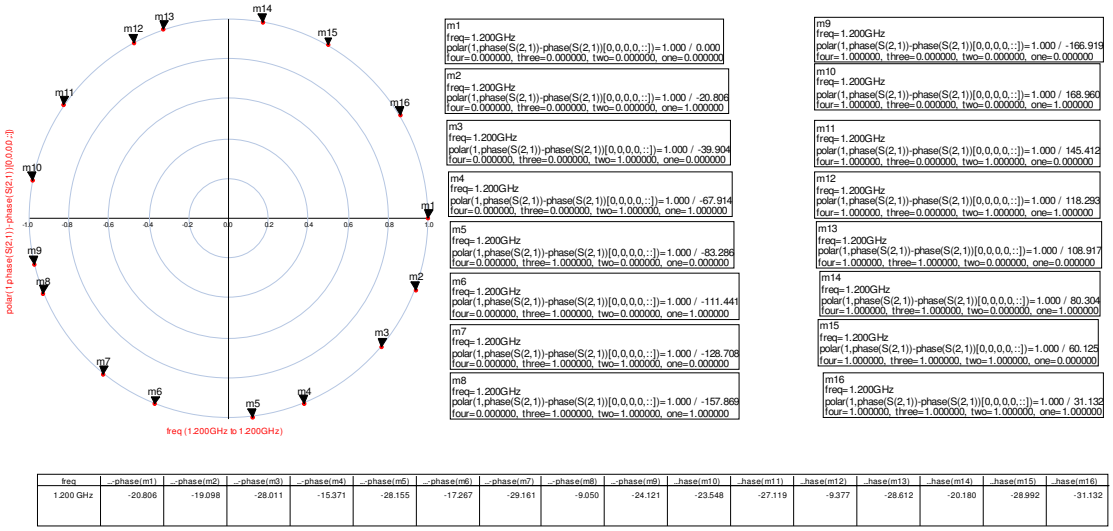
Figure 117: 180º bit insertion loss (left) & return loss (right) v. device size (number of fingers) for the reference state (red) and the phase shift state (blue)

5.1.7 4-Bit Phase Shifter Design

Figure 113 to Figure 117 demonstrate the simulated performance of each bit with all foundry models and terminated with 50 Ω. Each bit is designed to roughly give the required phase difference between the reference and phase shift paths when the bit is terminated with 50 Ω. Next, the bits were cascaded together to form two 4-bit phase shifters like Figure 101 inside the vector modulator of Figure 100. These cascaded bits perform differently than shown in Figure 113 to Figure 117 because the cascaded bits are not terminated by 50 Ω but rather by the impedances of another bit or the Wilkinson. The bits are cascaded so that those with the worst return loss are farthest away from each other, thus the order is 90º, 22.5º, 45º, 180º.

Since the bits have been designed for 50 Ω terminations, they must be adjusted to produce the correct phase shifts while terminated by the other bits (or the Wilkinsons). The performance of the individual phase shifters, within the vector modulator, may be simulated by connecting the same bits of each of the upper and lower phase shifters together. This results in 16 states with 1.7 dB variation in insertion loss, a return loss of better than 10 dB, and phase changes of 20.8º, 39.9º, 83.2º, 166.9º when each bit is on but the others are off.

The phases of all 16 states are shown in Figure 118, (with the magnitude not shown, i.e. all set to 1). Clearly the phase shifts of each of the 4 bits need to be adjusted since the 16 states are not equally distributed around 360º (the difference between states varies from 9º to 29º). The unequal distribution is due to the change in bit terminations described above.



freq	...phase(m1)	...phase(m2)	...phase(m3)	...phase(m4)	...phase(m5)	...phase(m6)	...phase(m7)	...phase(m8)	...phase(m9)	...hase(m10)	...hase(m11)	...hase(m12)	...hase(m13)	...hase(m14)	...hase(m15)	...hase(m16)
1.200 GHz	-20.806	-19.098	-28.011	-15.371	-28.155	-17.267	-29.161	-9.050	-24.121	-23.548	-27.119	-9.377	-28.612	-20.180	-28.992	-31.132

Figure 118: Phase states of cascaded bits before adjusting for non-50 Ω terminations

Initially, the easiest way to adjust the phase states to be more evenly distributed around 360º appeared to be adjusting each of the 4-bits directly, that is changing 20.8º, 39.9º, 83.2º, 166.9º by an additional 1.7º, 5.1º, 6.8º, 13.1º to achieve exactly 22.5º, 45º, 90º, 180º so that the 16 states are evenly spaced by 22.5º. Unfortunately, the solution isn't that simple. Adjusting each bit by only correcting the 22.5º, 45º, 90º, 180º phase states only considers when these bits are terminated by other bits in the off-state, but each of the 22.5º, 45º, 90º, 180º bits may not produce those phase

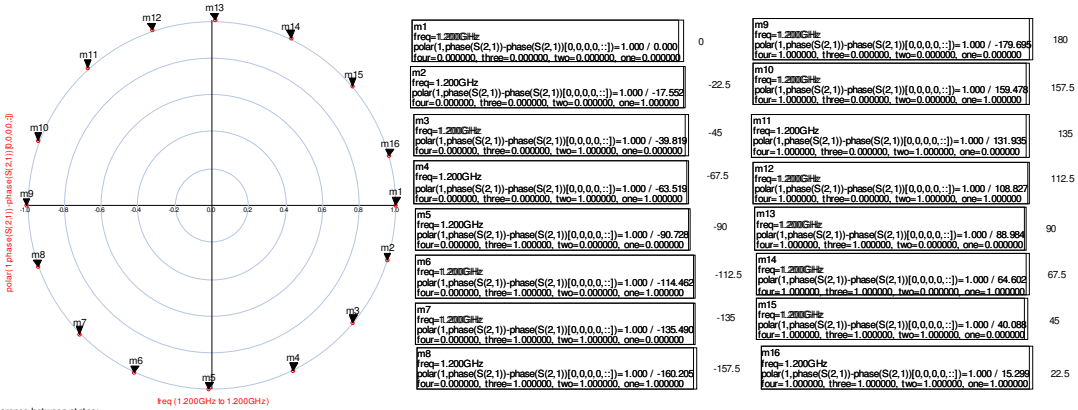
shifts when the other bits are on, which is required for the other 12 states. Indeed, *all* 16 states must be considered *simultaneously* when adjusting the *cascaded* bits for the desired 22.5º, 45º, 90º, 180º phase shifts. Therefore, instead of adjusting the π-network elements to achieve a particular phase shift for a single state, the π-network elements are *adjusted for even distribution* around 360º. This way the vector modulator will have states evenly distributed as well, which is required for deep null depths in an adaptive array. In fact, for deep nulls over the scanning range an even distribution of the states is more important than the absolute phase weight values for the adaptive array.

Since all of the states shown in Figure 118 seem a little lower than required, and the 180º bit is way off, the 90º/180º state was increased first. Therefore, new π-network element values were calculated to increase the 90º/180º bits by 6.8º/13.1º. This required changing the capacitor size to 59 µm wide by 60 µm long and also decreasing the inductance, which as achieved by solely changing the inductor size to x=y=358 µm. The new simulated phase shift was 90.7º/179.7º when tested with the 22.5º/45º bit off.

Next it appeared that the 22.5º bit should be reduced by about 2.5º. Although this would lower the 22.5º phase state further, when the 22.5º bit is used with the other bits it is actually producing more than 22.5º thus reducing the bit by 2.5º improves many states at the expense of one. Hence the capacitor size was changed to 25 µm wide by 26 µm long and the inductance was decreased by solely changing the inductor size to x=y=302 µm.

There didn't appear to be a need to adjust the 45º bit since changes to the 45º bit didn't appear to improve the distribution of the 16 states.

Simulation of the 16 phase states with the adjusted bits shows a more even distribution, as seen in Figure 119. With these adjusted bits, when the vector modulator is operated as a phase shifter, the input/output return loss is better than 10 dB and the insertion loss varies from 10 to 11.6 dB over the 16 states. This is shown in Figure 119 and Figure 120.



Difference between states:

freq	_phase(m1)	_phase(m2)	_phase(m3)	_phase(m4)	_phase(m5)	_phase(m6)	_phase(m7)	_phase(m8)	_phase(m9)	_hase(m10)	_hase(m11)	_hase(m12)	_hase(m13)	_hase(m14)	_hase(m15)	_hase(m16)
1.200 GHz	-17.552	-22.267	-23.701	-27.209	-23.734	-21.028	-24.715	-19.490	-20.827	-27.543	-23.108	-19.843	-24.382	-24.515	-24.788	-15.299

Deviation from perfect for each state:

freq	_phase(m1)	_phase(m2)	_phase(m3)	_phase(m4)	_phase(m5)	_phase(m6)	_phase(m7)	_phase(m8)	_phase(m9)	_hase(m10)	_hase(m11)	_hase(m12)	_hase(m13)	_hase(m14)	_hase(m15)	_hase(m16)
1.200 GHz	0.000	-4.948	-5.181	-3.981	0.728	1.962	0.490	2.705	-0.305	-1.978	3.065	3.673	1.016	2.898	4.912	7.201

Figure 119: Evenly distributed phase states of the cascaded bits after adjustment

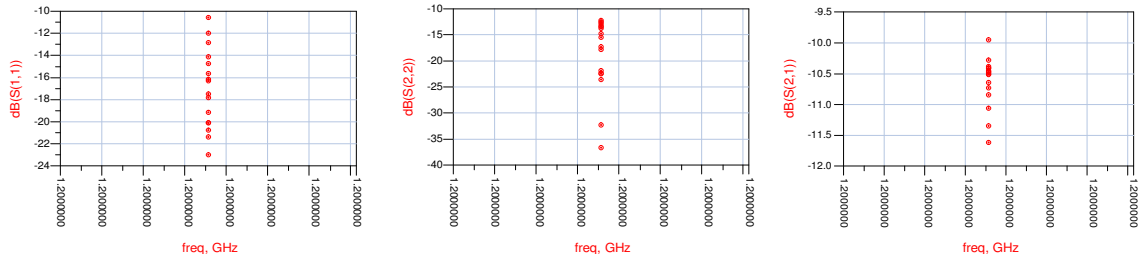


Figure 120: Input return loss (left), output return loss (centre) and insertion loss (right) of the vector modulator when operated as a 4-bit phase shifter (16 states only)

5.1.8 4-Bit Vector Modulator Design

With the bits fully adjusted to be evenly distributed around 360º, all 256 states of the 4-bit vector modulator were simulated. These results, shown in Figure 121, demonstrate an input/output return loss of at least -10 dB and a relatively even distribution of the 256 states. Weights with up to 50dB of amplitude variation between 0º and 360º are possible.

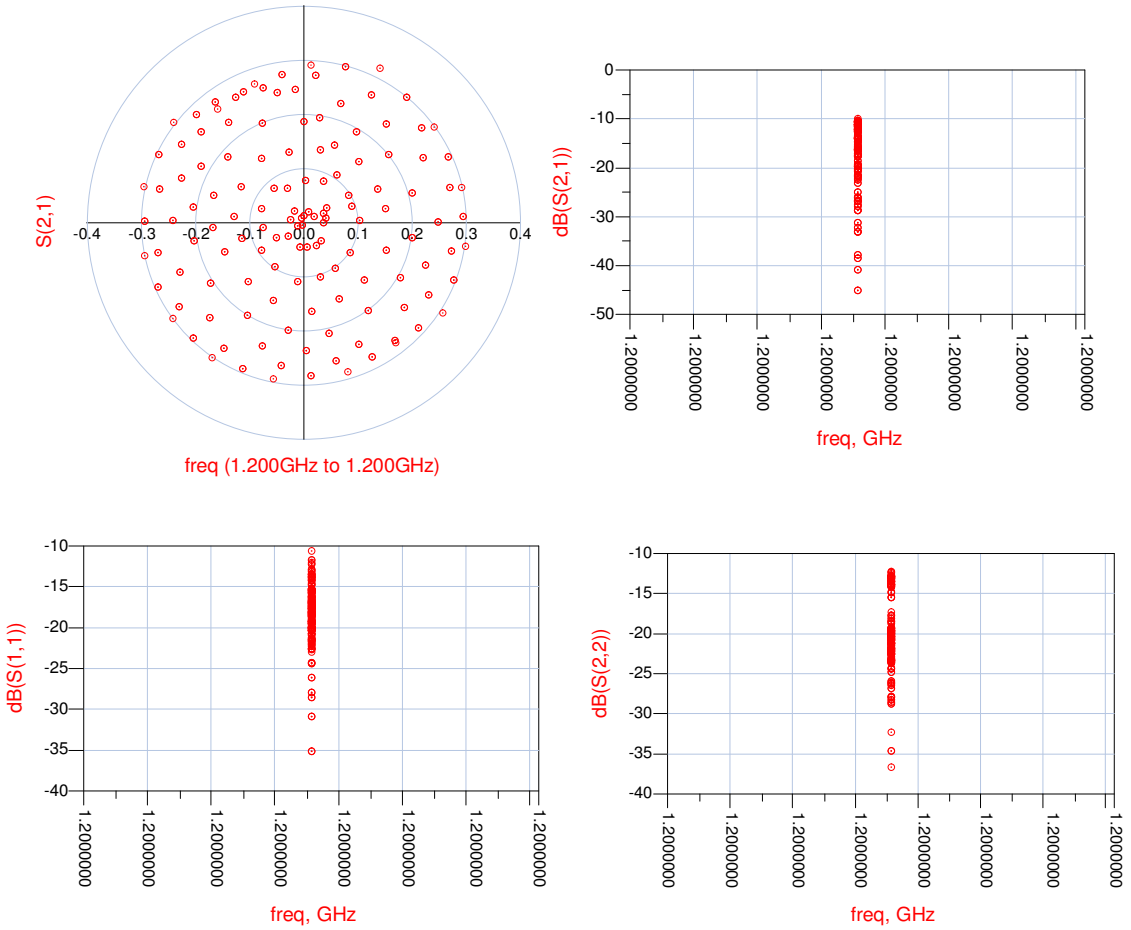


Figure 121: Simulated 4-bit vector modulator (all 256 states)

5.1.9 Layout and Interconnects

The vector modulator design was laid out using a combination of Mentor Graphics schematic driven layout and Agilent ADS. The lumped elements and transistors were interconnected using 50 Ω thin film microstrip (TFMS) lines. The design uses TFMS with the signal line on the top metal layer and the ground on the bottom metal layer. The maximum ground plane width is limited to avoid the need for stress relief slits. The ground plane is solely used under the interconnecting TFMS lines; there is no ground plane under the lumped elements nor within 10 µm of any lumped element because the lumped element models from the foundry do not include a ground plane.

Once the interconnecting lines were determined, they *all* were included in the schematic using MLIN microstrip ADS models and the vector modulator was re-simulated. Since the interconnecting lines within each bit were kept small, their impact on the vector modulator performance was also small. The simulated results of the vector modulator including microstrip interconnect models is shown in Figure 122. These results are very similar to the simulations without interconnects shown in Figure 121.

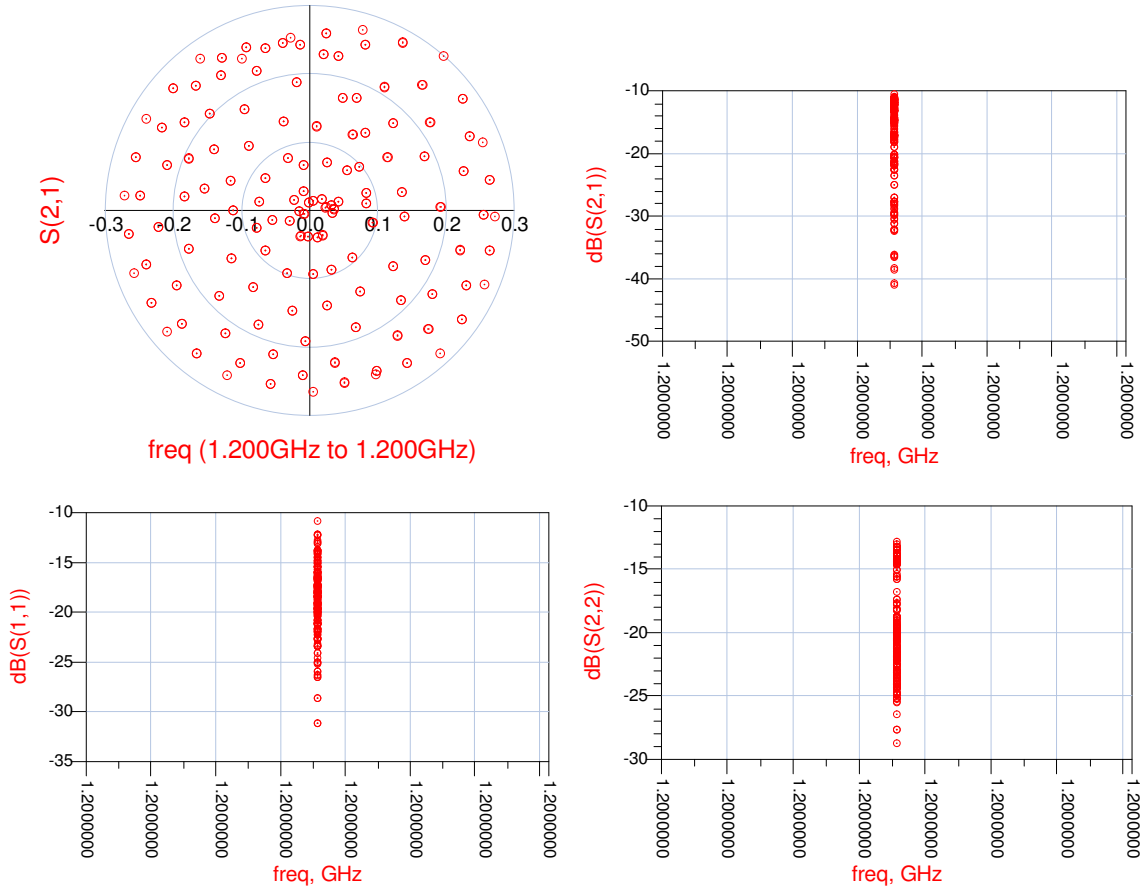


Figure 122: Simulated 4-bit vector modulator (all 256 states) with microstrip interconnects

5.1.10 Fabrication

The 4-bit vector modulator was fabricated by the foundry. A photograph of the completed circuit is shown in Figure 123 and it measures 4 mm 1.5 mm.

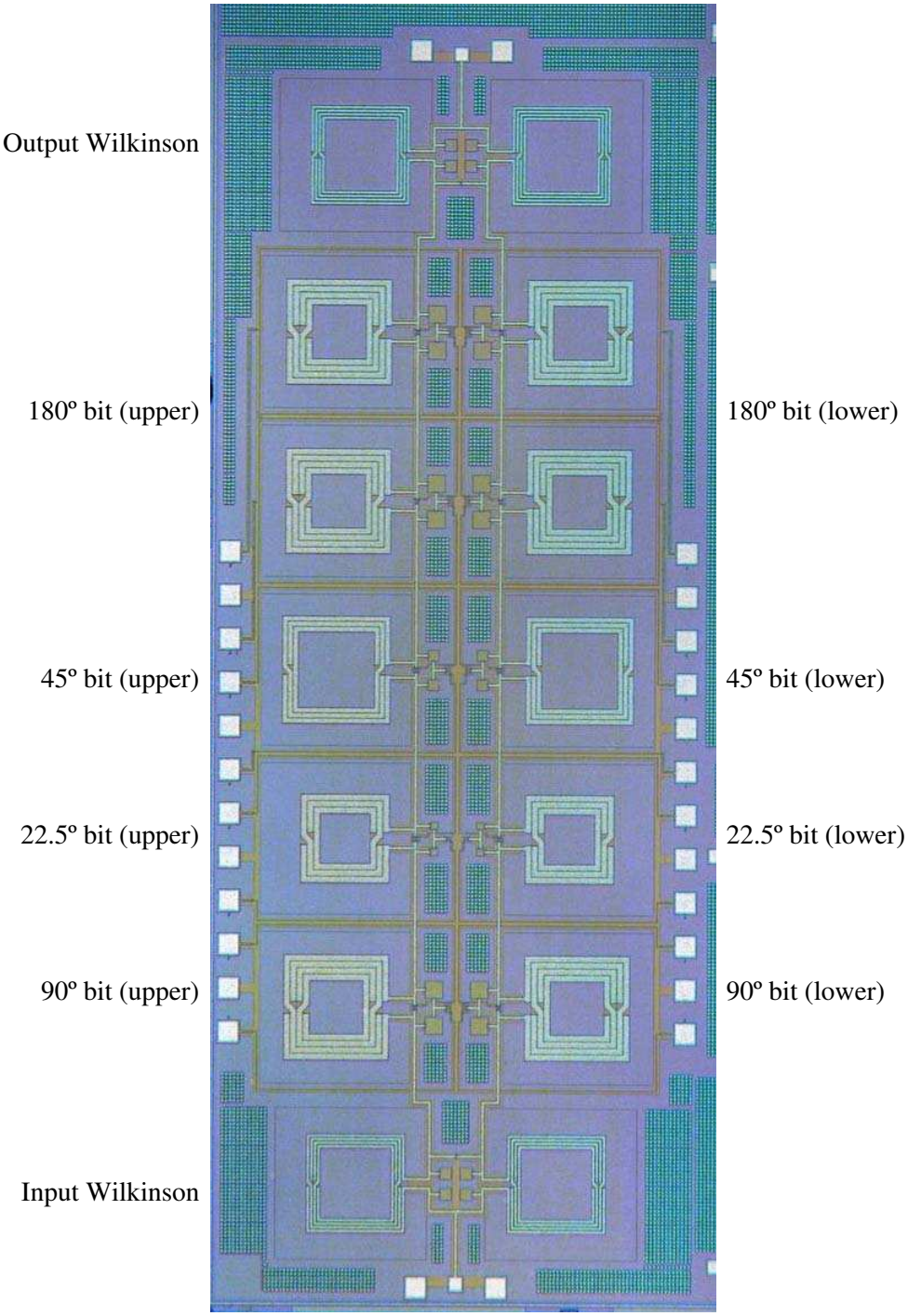


Figure 123: Photograph of the fabricated 4-bit vector modulator

5.1.11 Measurement Performance as a Phase Shifter Only

The fabricated vector modulator was first tested with the corresponding bits of both the upper and lower phase shifters connected together. When connected in this configuration, the vector modulator does not alter the amplitude of the input signal and thus operates as if it were a single phase shifter. The advantage of testing the vector modulator in this configuration is that the various combinations of the bits can be tested.

The vector modulator was measured on-wafer using coplanar probes and open-short-load-thru calibration to the probe tips. The measured input/output return loss, insertion loss and insertion phase shift of each of the 16 states is shown in Figure 124.

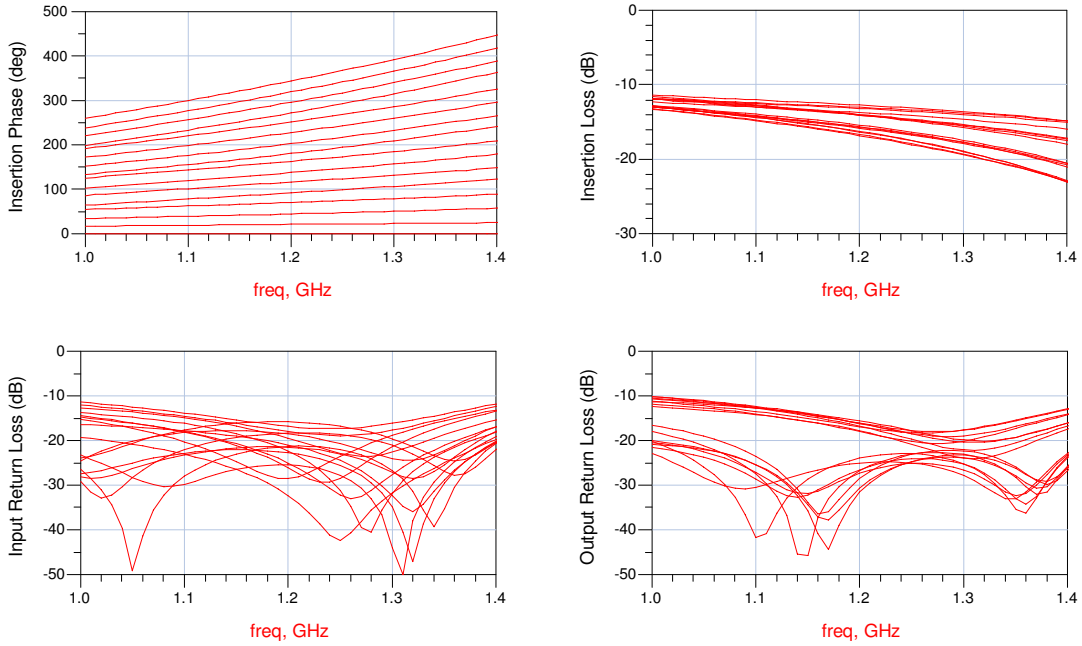


Figure 124: Measured performance of the 4-bit vector modulator operated as a phase shifter only

Figure 124 shows that while the desired phase shifts are evenly distributed, some of the states have more loss than others. At 1.2 GHz, the insertion loss varies from about 13 dB to 16.5 dB. This is mainly due to the 180º bit which is, in fact, two 90º bits in series, and thus the extra loss is expected, and is perhaps more easily seen in the polar plot of S_{21} shown in Figure 125 where the magnitude of S_{21} is less for states involving the 90º and 180º bits. Figure 126 also shows that the insertion loss increases when the 90º bit is used, and then again when the 180º bit is used.

The measured phase shift of each state, when the 4-bit vector modulator is operated as a phase shifter only, is shown in Table 1. Simulated results are also shown for comparison.

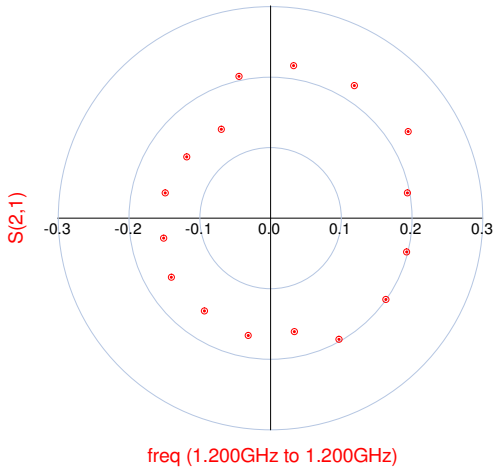


Figure 125: Measured S_{21} of the 4-bit vector modulator operated as a phase shifter only

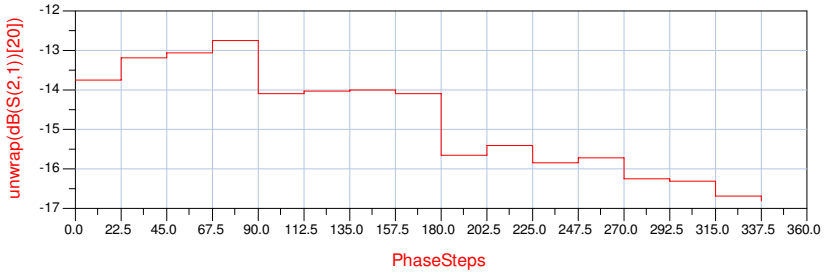


Figure 126: Measured insertion loss of the 4-bit vector modulator (operated as a phase shifter only) as a function of the phase shift states

Table 1: Measured phase shift of each state of the 4-bit vector modulator when operated as a phase shifter only. Simulated results are also shown for comparison.

State	Ideal phase shift (deg)	Measured phase shift (deg)	Simulated phase shift (deg)
0	0	0	0
1	22.5	21.2	17.6
2	45	44.5	39.8
3	67.5	70.3	63.5
4	90	92.0	90.7
5	112.5	116.2	114.5
6	135	137.6	135.5
7	157.5	163.0	160.2
8	180	180.3	179.7
9	202.5	202.8	200.5
10	225	227.5	228.1
11	247.5	251.4	251.2
12	270	271.5	271.0
13	292.5	295.9	295.4
14	315	318.8	319.9
15	337.5	343.6	344.7

Although Table 1 shows the measured v. ideal phase shift for each state, two figures of merit that are often cited for phase shifters are the RMS phase error, $\theta_{\Delta,\mathrm{RMS}}$, and the RMS amplitude error, $A_{\Delta,\mathrm{RMS}}$, defined in (7) and (8). For $N=16$ digital input states, $\theta_{\Delta i}$ is the ith output phase error from the ideal phase value of the ith digital input state. The $A_{\Delta i}$ is $A_{\Delta i} = A_{vi}(\mathrm{dB}) - A_{ave}(\mathrm{dB})$ where A_{vi} is the ith S_{21} in dB corresponding to the ith digital input state and A_{ave} is the average S_{21} in dB of all $N=16$ states. At 1.2 GHz, the measured RMS phase error, $\theta_{\Delta,\mathrm{RMS}}$, and the measured RMS amplitude error, $A_{\Delta,\mathrm{RMS}}$, are

$$\theta_{\Delta,\mathrm{RMS}} = \sqrt{\frac{1}{N-1}\times\sum_{i=2}^{N}\left|\theta_{\Delta i}\right|^2}\,(\mathrm{deg}) = 3.197^\circ \tag{7}$$

$$A_{\Delta,\mathrm{RMS}} = \sqrt{\frac{1}{N}\times\sum_{i=1}^{N}\left|A_{\Delta i}\right|^2}\,(\mathrm{dB}) = 1.332\,\mathrm{dB} \tag{8}$$

5.1.12 Measured Performance of the Full 4-bit Vector Modulator

All 256 states of the 4-bit vector modulator were tested, on wafer, using a combination of:

an Agilent 16702B Pattern Generator/Logic Analyzer,

an Agilent N5250A Network Analyzer, and

a Tektronics AFG320 Arbitrary Function Generator.

The Pattern Generator was used to generate the 8 digital inputs, 4 for each phase shifter, resulting in a total of 256 states. Each phase shifter bit also requires the complement of its digital input, and thus the Pattern Generator was also used to generate 8 bits that are the complement of the digital input states. Each output bit from the Pattern Generator was 0V for a low and 2.5V for a high. The vector modulator was designed and simulated for a high of 3.3V; however, only 2.5V pod connectors were available. Simulations using a 2.5V high did deviate slightly from simulations with a 3.3V high, however the 2.5V simulations still showed that the vector modulator can produce the desired 256 amplitude and phase weight combinations.

The lowest setting for the internal clock of the Logic Analyzer, which dictates the period between the states, is 4 kHz. This is too fast for the Network Analyzer to perform a frequency sweep and save the measured s-parameters. Therefore, the Arbitrary Function Generator was used to produce a 0.4 Hz, 3V square wave that was used as an external clock for the Pattern Generator. This resulted in about a 3 second period between states, which was more than enough for the Network Analyzer to perform a frequency sweep and save the s-parameters.

An Agilent data logger utility was used to automatically save the measured s-parameters for each state in data files with incremental file names. The resulting 256 s-parameter data files were then read into Agilent ADS using “DAC controlled file steering”. ADS sequentially stepped through a text file listing all of the data file names thus allowing the measured s-parameters to be parameterized by both frequency and state. Figure 127 shows that the measured input and output

return loss of the 4-bit vector modulator, for all of the 256 possible states, is better than 10 dB over the entire measured frequency range.

At 1.2 GHz, the measured amplitude and phase weights for all 256 possible states of the 4-bit vector modulator are shown in Figure 128. In terms of insertion loss, this corresponds to a measured range of -13.4 to -32.8 dB at 1.2 GHz. Compared to the simulated 256 states shown in Figure 122, the measured states in Figure 128 are compressed slightly on the left side. There is also a small gap in the measured states to the left of the origin and those states on the right of the origin are also slight compressed compared to the same area in Figure 122. These differences are primarily due to the 90º and the 180º bits having more loss than predicted by the simulations (see also discussion in the previous section). This was confirmed by simulating a 4-bit vector modulator using all ideal phase shifters, switches, and Wilkinsons, as shown in Figure 129. Since the measured S_{21} of the reference (0º) state was -14 dB and 100º, an ideal 14 dB attenuator and an ideal 100º phase shift was included in the input to apply to all simulated states.

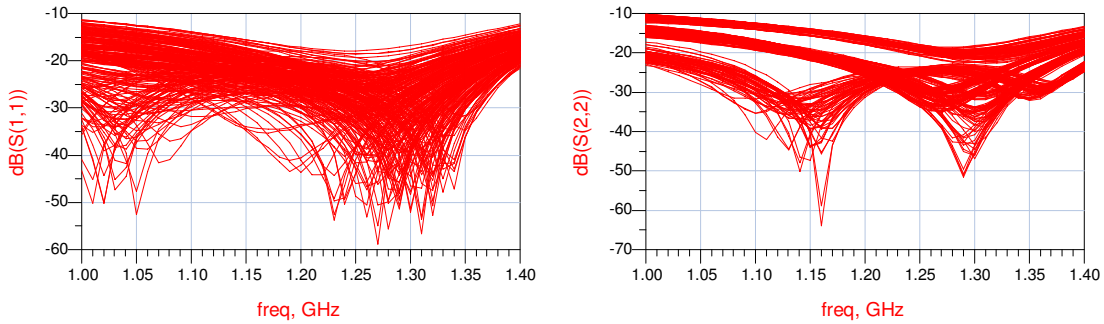


Figure 127: Measured input return loss (left) and output return loss (right) of all 256 possible states of the 4-bit vector modulator

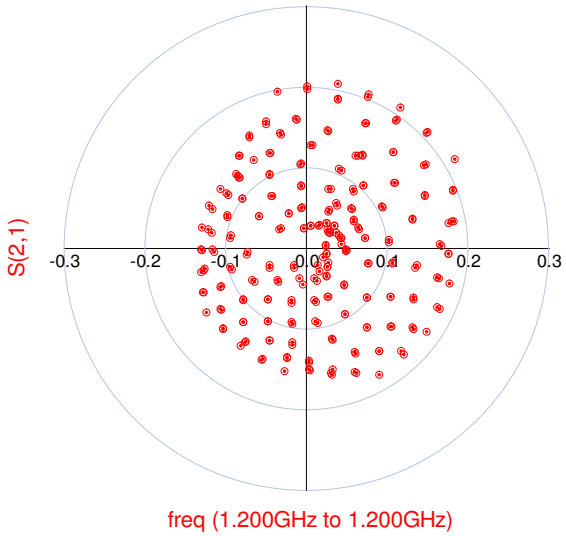


Figure 128: Measured amplitude and phase weights (S_{21} of all 256 possible states) of the 4-bit vector modulator

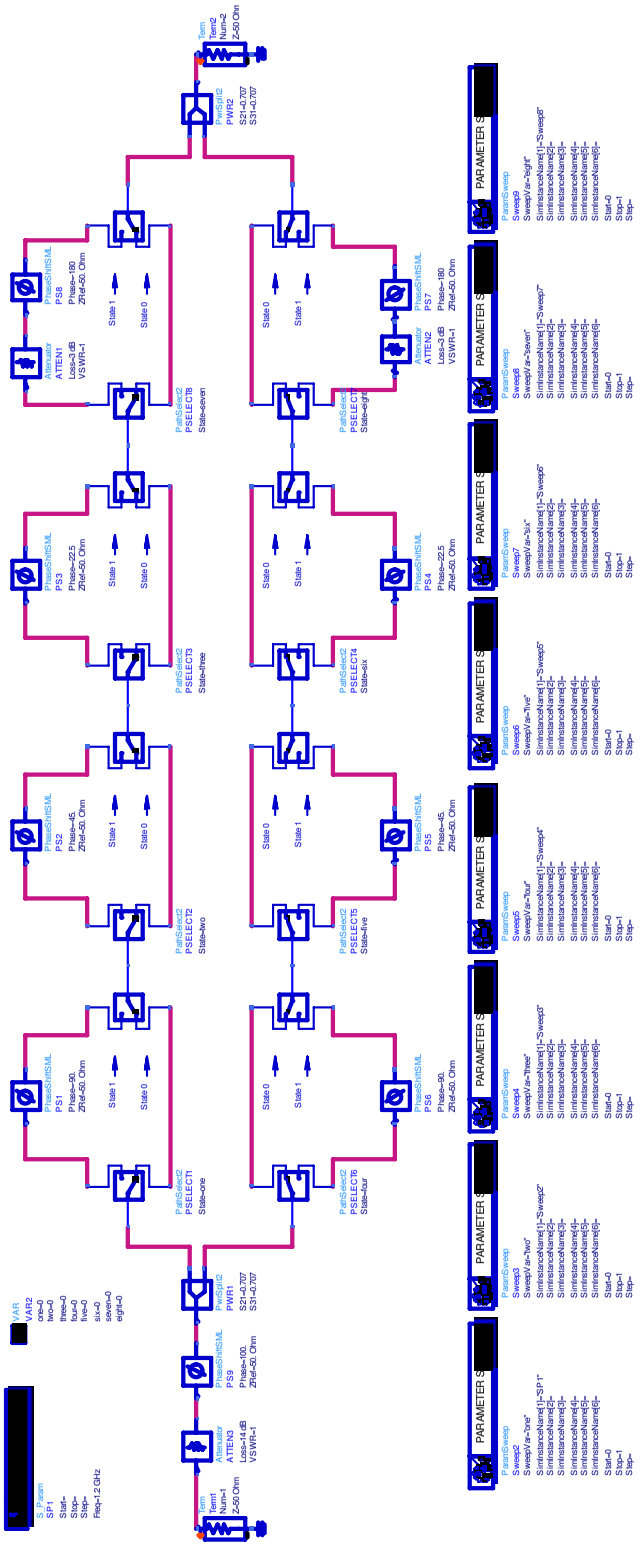


Figure 129: Idealized 4-bit vector modulator with extra loss in the 180º bit

The 90º, 45º, and 22.5º phase shifts in Figure 129 are ideal and lossless; however, the ideal 180º phase shift includes an additional 3 dB attenuator to account for the extra loss in the actual 180º bit compared to the other bits. Without this additional loss, the vector modulator states are ideal and shown in Figure 130. When the extra 3 dB of loss is included in the 180º bit, the simulated states of the idealized vector modulator are shown in Figure 131 (left), and this correlates closely to the measured results shown in Figure 131(right) for comparison. Therefore, the difference between the measured 4-bit vector modulator performance and the simulated/ideal performance can be mostly attributed to the extra loss of the 180º bit. As mentioned previously, this extra loss is not unexpected since the 180º bit comprises two 90º bits and should naturally have more loss than the other bits.

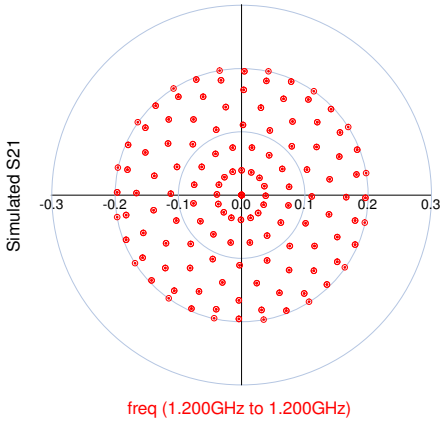


Figure 130: Idealized vector modulator simulation without extra loss in the 180º bit

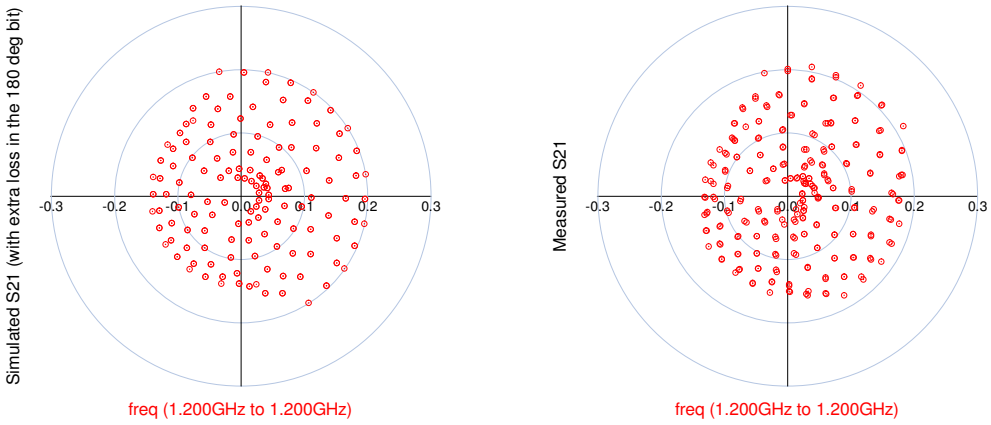


Figure 131: Idealized vector modulator with additional loss in the 180º bit (left) compared to the measured states of the fabricated 4-bit vector modulator (right)

5.2 5 GHz Analog Phase/Amplitude Control

5.2.1 Phased Array Architectures and Phase Shifters

There are a number of different phased-array architectures, differing in where the phase shift is inserted in the receive/transmit chain. The four different options from Figure 97 are illustrated again for convenience in Figure 132. The first option is to insert the phase shift in the radio frequency (RF) path (Figure 132(a)), which has the advantage of minimal power consumption and area, since only the antennas and phase shifters (and variable gain amplifiers if it is necessary to adjust the amplitude of each path) must be duplicated, and the intermediate frequency (IF) and baseband stages can be shared between all signal paths. Another advantage is that since the interferes are nulled out at the RF stage, linearity requirements on the IF/baseband stages can be relaxed.

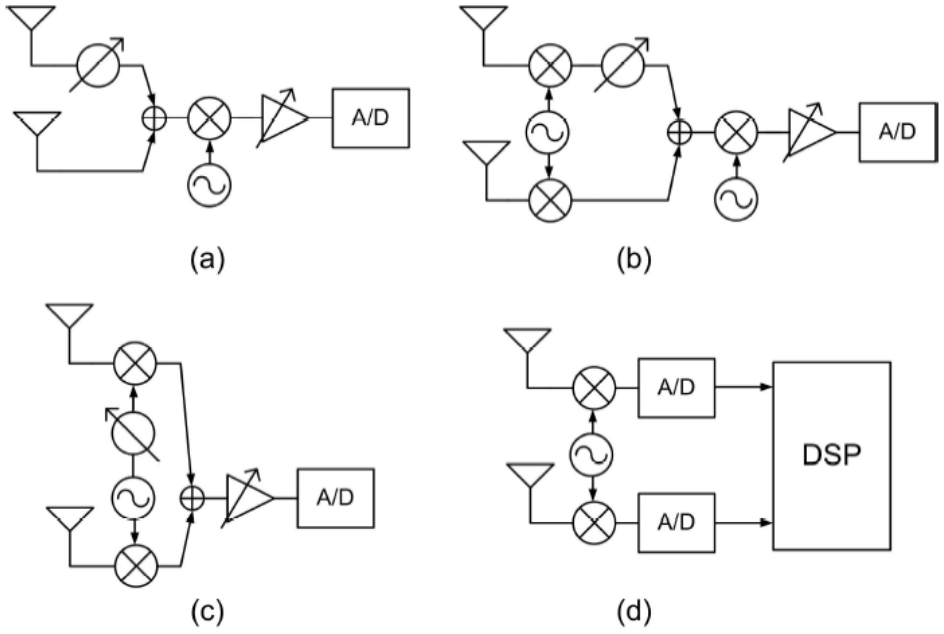


Figure 132: Possible architectures for implementing a phase shift in a multiple antenna receiver

The second option is to insert the phase shift at the IF stage (Figure 132(b)), which is desirable from the standpoint that it is easier to realize accurate phase shifts at lower frequencies. Some disadvantages of this approach are that there will be increased power and area consumption due to increased duplication (now each antenna path requires a dedicated mixer for the downconversion to IF) and the phase shifters themselves will be larger since the passive components required in a phase shifter scale in inverse proportion to the frequency of operation, so inductors and capacitors will be larger than they would be if the phase shifter was operating at RF.

The third option is to apply the phase shift to the local oscillator (LO) signal before it is applied to the mixer (Figure 132(c)). This scheme will have a power consumption between that of the RF

and IF phase shift architectures. It is attractive since it relaxes the requirement for the phase shifter to have constant amplitude for varying phase shifts. Since the mixers are typically hard driven, the LO stages are operated in saturation, and variation in the phase shifter output will have a reduced impact. A disadvantage of this scheme is that the time delay is not applied to the modulated signal, so for very wideband signals some distortion will be introduced; however, for almost all communication systems the bandwidths are such that the delay is negligible in the modulated signal.

The fourth option is to add an analog to digital (A/D) converter to each path and perform the phase shift and any other required manipulation in the digital domain (Figure 132(d)). This is an attractive option from a flexibility standpoint, as the receiver/transmitter could be reconfigured for any of the multiple input/multiple output (MIMO) techniques that have been discussed. However, the additional A/D converters (one for each antenna) greatly increase the power consumption, and it is difficult to design A/D converters with adequate performance as the linearity, dynamic range, and speed requirements are very stringent.

The phase shifter is at the very heart of a phased array antenna, and beam-steering performance is directly tied to the phase performance of the phase shifter. Generally, the phase performance of a phase shifter is related to its insertion loss. When phase error is extremely important (i.e., military radar), insertion loss can be overcome with additional amplification for an increase in cost and power consumption.

There are a number of general requirements for a phase shifter to be used in a multiple antenna beam steering system. The phase shifter should be compact and consume minimal power (if an active topology is chosen), since the number of phase shifters scales in proportion to the number of antennas in the system. Smaller phase shifters allow more antennas to be incorporated into the system, and reduced power consumption extends the battery life in portable applications. The phase shifter should also have a low noise figure (NF) and minimal loss.

Another requirement is that the phase shift should be approximately constant over the signal bandwidth, to minimize distortion effects, which lead to increased bit error rate (BER) in the case of communications applications. In most architectures it is important for the phase shifter to have constant gain or loss (depending on phase shifter type) across the phase shift range.

Finally, the phase shifter must provide at least 180° of phase shift with high resolution. It would be preferable to have 360° of phase shift, but if only 180° is available then the full range can still be covered through switching a fully differential signal. The switches required in this situation will introduce additional losses to the signal, so this is less desirable than having a full 360° of phase shift. Phase shift ranges of less than 180° and limited phase resolution both limit the effectiveness of the beam steering. With these requirements in mind, different phase shifter topologies can be compared. The most well known architectures are switched high-pass/low-pass (HP/LP) filters, reflective-type phase shifters, all-pass filters, and vector modulators.

5.2.1.1 High-Low Pass Phase Shifter

The High-Low Pass phase shifter (Figure 133) was first introduced over 30 years ago. The original advantage of this phase shifter was its superior power and phase bandwidth capabilities. The high-low pass phase shifter functions by taking the difference between the phase from a high

pass filter path and the phase of a low pass filter path for each bit. Each individual bit will have independent high and low pass paths, with single pole, double throw (SPDT) switches on both sides of the bit (Figure 133). These filters are specifically designed for both very small loss in the band of operation and a linear phase response, which is set to either advance or delay the phase by half the desired amount, depending on which path is selected.

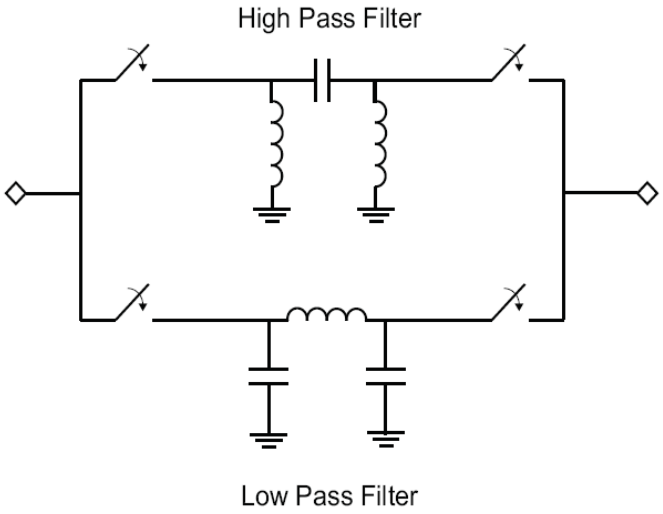


Figure 133: A single bit in a switched line phase shifter

Because this topology does not depend on specific transmission line lengths, a constant phase shift over a bandwidth of more than an octave can be achieved. This is possible because the phase response of both the high and low pass paths behaves similarly when moving away from the center frequency, causing a constant difference in phase between the two paths.

In the past five years, there has been a renewed interest in the use of the high-low pass shifter topology, particularly in SiGe integrated circuit designs targeting monolithic transmit/receive (T/R) module applications for phased array radar. From simple bit topologies with p-i-n diode switches, to more complicated designs, the high-low pass phase shifter has been found to be an ideal architecture because of its small size, flat phase response over a broad bandwidth, and its ability to cancel out phase effects from switches and routing schemes.

However, inherent device limitations in silicon-based (e.g., SiGe) monolithic design approaches make achieving optimal phase performance difficult. Only a narrow range of inductor and capacitor values may be fabricated, complicating bit designs for a given band of operation. The inductors pose additional challenges because of their higher parasitics in silicon technology, resulting in lower Q and self-resonance frequencies. SPDT switch performance may also increase the phase variation associated with a given shifter. The phase performance of a single bit can additionally influence the phase of adjacent bits, leading to integration challenges and a degradation of overall shifter performance.

5.2.1.2 Analog Reflective-Type Phase Shifters

A reflective type phase shifter (RTPS) consists of a hybrid 90° coupler combined with two reflective loads. The operation of an RTPS is illustrated in Figure 134. The incoming signal is split evenly into two parts, with one part of the signal experiencing a 90° phase shift relative to the other. Each part of the signal is then reflected by a load with a different input impedance than the coupler, introducing an additional phase shift (φ). This phase shift is equal to the phase of the reflection coefficient, which is expressed as:

$$\Gamma = (Z_L - Z_0)/(Z_L + Z_0) \tag{9}$$

where Z_L is the load impedance and Z_o is the characteristic impedance.

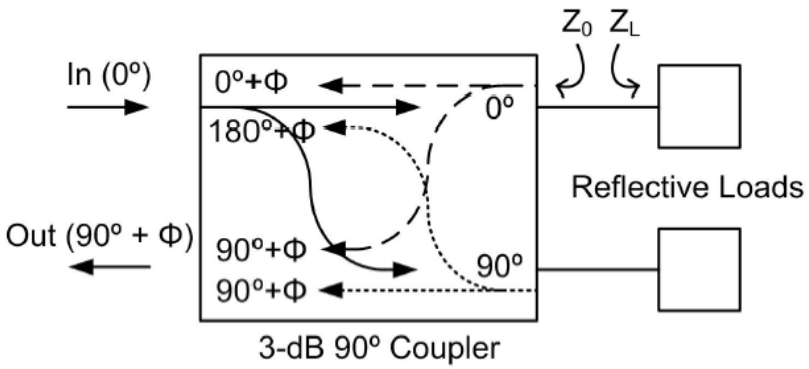


Figure 134: An analog reflective-type phase-shifter

The reflected signals are then split and phase shifted again by the coupler, so that the signal components emerging from the input port are 180° out of phase and cancel each other. The signals emerging from the output port are in phase and combine constructively, with a total phase shift of 90°+φ. The phase shift is varied by incorporating a varactor into the reflective load, allowing the input impedance to be changed, thereby changing the phase shift.

Implementing this phase shifter in a silicon process, which may lower the cost, presents a number of design challenges such as the increased losses due to the conductive substrate and the lower quality integrated passives. Nevertheless, there are techniques for reducing these losses to achieve losses approaching those of designs on semi-insulating substrates like GaAs. For example, active components may be used to compensate for the losses of integrated silicon inductors.

An example of a lumped element implementation of a RTPS is shown in Figure 135.

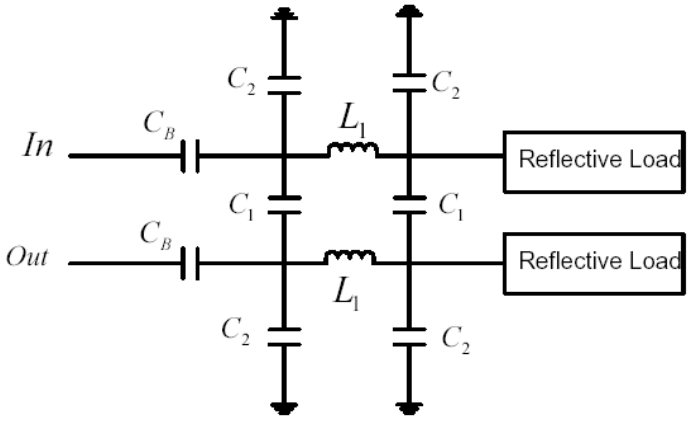


Figure 135: Lumped element, reflective-type phase shifter

5.2.1.3 Phase and Amplitude Control Using Polar Modulation

The most accurate and reliable amplitude and phase control can be obtained using digital signal processing (DSP) and direct-digital synthesis (DDS) techniques; however their increased hardware complexity do not make these techniques the most cost-effective solutions for implementing large phased arrays.

Polar modulation on the other hand, although being an analog technique, employs a simple operation principle that can be used to implement a low cost phase shifter producing reliable results. Polar modulation is a technique whereby an arbitrary signal, or carrier, can be time-varied in both magnitude and phase by controlling the magnitude of its in-phase and quadrature components. The simplest way to explain this concept is by means of a sinusoidal signal, $\cos(\omega_o t)$, whose in-phase and quadrature components are $\cos(\omega_o t)$ and $\sin(\omega_o t)$ respectively. Suppose we have these two signal components and we are going to inject them into the hardware shown in Figure 136, then the output of this diagram is given by (10).

$$g(t) = I(t)\cos(\omega_o t) + Q(t)\sin(\omega_o t) \tag{10}$$

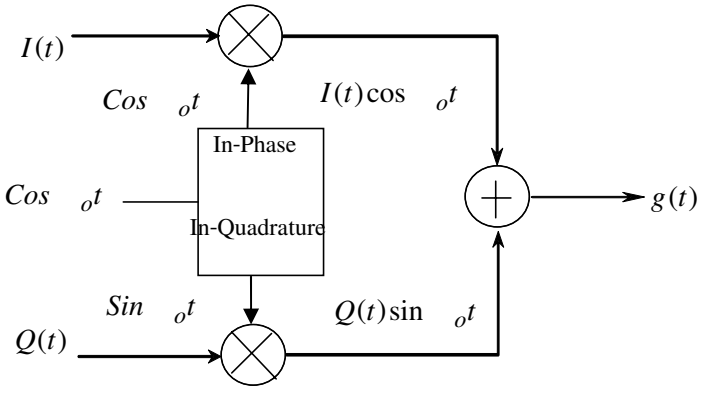


Figure 136: Vector modulator

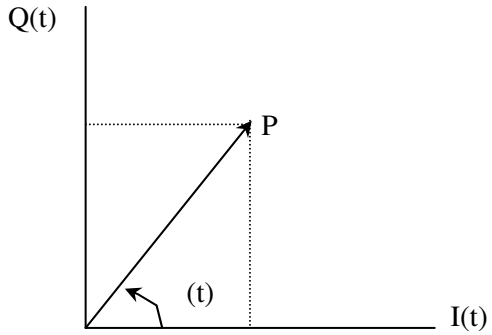


Figure 137: Phasor representation

We can represent the signal as a phasor with magnitude r(t) and phase θ(t). From Figure 137 we can easily convert polar coordinates r(t) and θ(t) to rectangular coordinates I(t) and Q(t) using equations (11) and (12), that is, by projecting the point P onto the I and Q axes (in-phase and quadrature, respectively):

$$I(t) = r(t)\cos(\theta) \tag{11}$$

$$Q(t) = r(t)\sin(\theta) \tag{12}$$

It is possible to convert rectangular coordinates I(t) and Q(t), to polar coordinates r(t) and θ(t) using equations (13) and (14).

$$r(t) = \sqrt{I^2(t) + Q^2(t)} \tag{13}$$

$$\theta(t) = \tan^{-1}\left(\frac{Q(t)}{I(t)}\right) \tag{14}$$

Substituting (11) and (12) in to (10) and then using a trigonometric identity yields,

$$g(t) = r(t)\left[\cos(\theta(t))\cos(\alpha_o(t)) - \sin(\theta(t))\sin(\alpha_o(t))\right] \tag{15}$$

$$g(t) = r(t)\cos\left[\alpha_o(t) - \theta(t)\right] \tag{16}$$

Note that by controlling the weighting signals *I(t)* and *Q(t)* we can achieve magnitude and phase control of the output signal.

To drive the I and Q weighting signals, two differential 16-bit digital-to-analog converters can be used to provide high resolution. This concept can be easily applied to the development of a phase shifter for high frequency applications, which is attractive for designing phased array radars.

5.2.2 Analog Phase/Amplitude Control Topology

There are an increasing number of electronic warfare applications requiring adaptive phased arrays having tight illumination tolerances for both shaped and low side lobe beams. Continuous phase and amplitude control capability can reduce the individual circuit tolerance requirements by providing in situ circuit trimming through the use of automated near field measurements. Continuous phase shifters using dual gate FET amplifiers or variable PIN attenuators for vector amplitude control have been described in the literature. A potentially compact phase/amplitude control module based on a vector modulator is described in this section.

5.2.2.1 90° Vector Modulator Phase Shifter

5.2.2.1.1 Principle of the Phase Shifter

The key element of a 360° phase shifter is an analog 90° phase shifter employing two cascode low-noise amplifiers (LNAs). The conceptual design of the 90° phase shifter is shown in Figure 138. The two amplifiers are excited in phase quadrature through a hybrid power splitter at a designated frequency. The outputs of both amplifiers are then combined through an in-phase power combiner to produce a phase-controlled output.

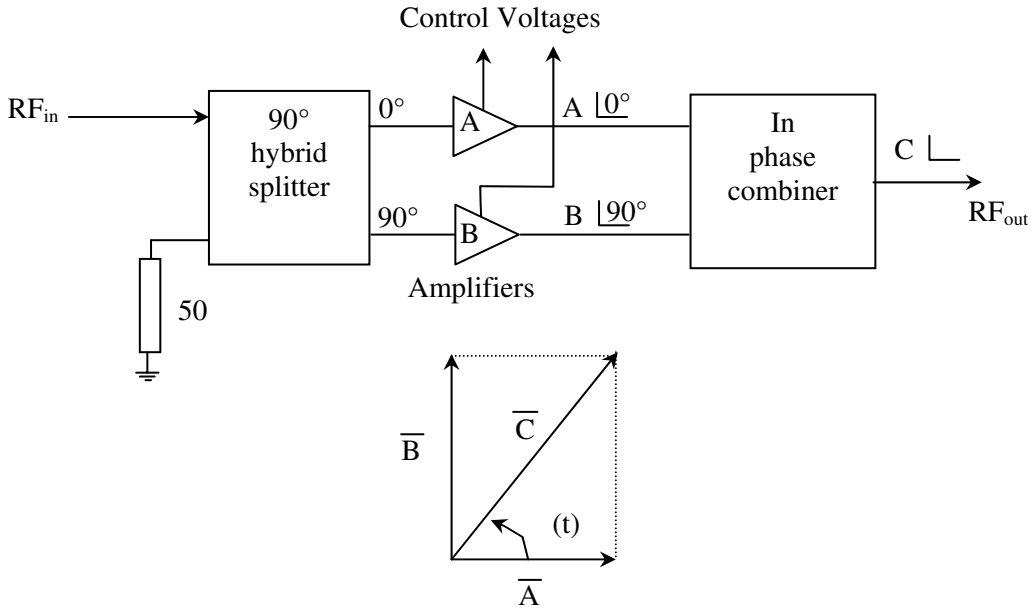


Figure 138: Schematic of a 90° SiGe analog phase shifter

The two cascode LNAs are used as variable gain amplifiers. The gain of the cascode amplifiers can be controlled from +15 to –15 dB by controlling the second base bias voltage. The phase difference in path A and path B in Figure 138 is 90°. The resulting vector sum of the two combined quadrature RF signals is given by:

$$C = A + B$$
$$C\angle\phi = A + jB = |C|\angle \tan^{-1} {}^{B}\!/_{A} \tag{17}$$

where C is the resultant RF voltage amplitude and is the phase angle. The output phase angle is, therefore, controlled by adjusting the relative amplitudes of the quadrature vectors A and B. This is accomplished by independently adjusting the gain of each of the cascode amplifiers. For most system requirements, the absolute amplitude of the resulting phase shifted RF signal must be kept constant and independent of the selected output phase angle. This means that |C| is invariant and the phase angle is selected by controlling the amplitudes of both RF signals A and B. For this unique requirement:

$$|C| = \sqrt{A^2 + B^2} = \text{Constant} \tag{18}$$

The overall amplitude of the phase shifter can be varied by changing the base voltages of both amplifiers simultaneously. Thus in (18), the constant output amplitude level can be varied and this phase shifter becomes a vector generator. A vector generator is a device where a vector of any phase or amplitude (with respect to an input reference signal) can be generated.

5.2.2.1.2 Design of a Variable Gain Amplifier (VGA)

There are several VGA design approaches that can be implemented in SiGe technology. One approach is based on the bias dependent characteristics of the transistor's transconductance G_m. The variable gain is realized by controlling the quiescent current of the transistor to change the device G_m. This has the advantage of being able to selectively obtain low dc power dissipation and low noise figure. The disadvantages are that the linearity (IP3) and output power characteristics are strongly dependent on the quiescent bias current of the transistor, and the gain control range is limited (15 dB).

The 5 GHz cascode LNA outlined in Section 3.1 was used as a VGA by using bias for gain control. Figure 139 shows the circuit topology and the biasing technique for this variable gain amplifier. The gain can be monotonically decreased by decreasing the control voltage V_{b1} while keeping the two other bias voltages (V_b,V_c) constant. The gain is decreased since the transconductance of the transistors decreases with the decreasing base bias current. This bias control method has the advantage that the control current (base current) is very low.

The simulated gain, NF and input/output return loss of the cascode VGA were characterized versus the corresponding bias voltage. Figure 140 shows the wideband variable gain response from 4 GHz to 6 GHz at various voltage V_{b1} levels. The plot illustrates over 35 dB of gain control. The gain flatness is less than 2 dB over the full 4-6 GHz frequency band and 35 dB gain control range. The maximum attenuation is determined by the parasitic input-to-output feedback capacitance of the transistors. Due to the small size of the transistors, the values of these feedback capacitances are low. Consequently, high gain-control ranges of above 35 dB are achieved. Figure 141 shows the simulated gain as a function of control voltage V_{b1} at 5 GHz. The gain

control is fairly linear over a 25-dB range. The total available gain control range is >35 dB. Figure 142 and Figure 143 show the input and output return loss, respectively, versus V_{b1} voltage.

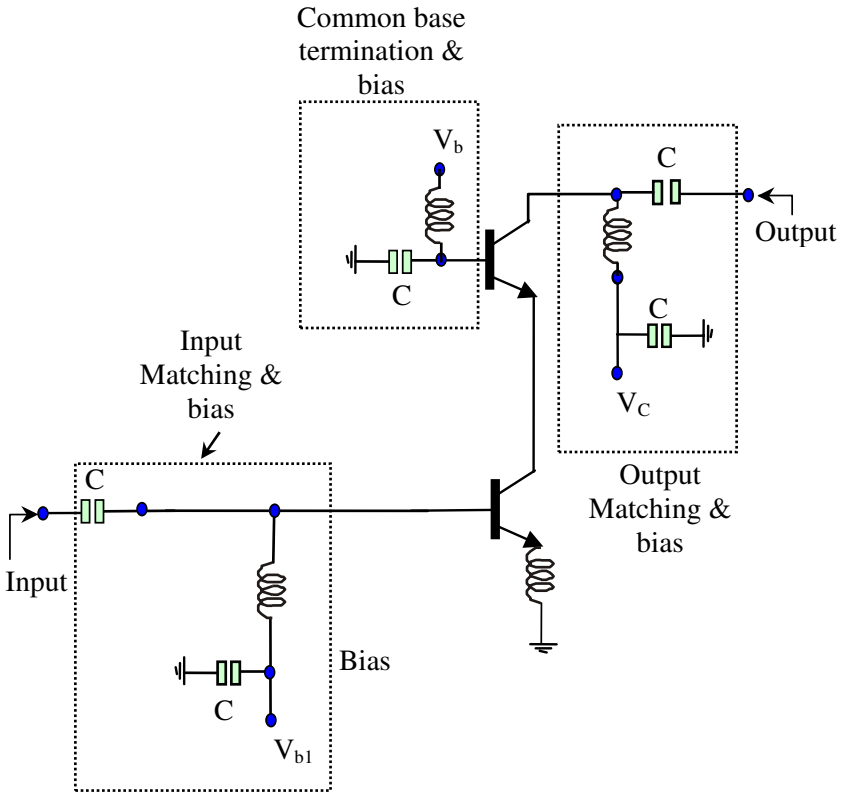


Figure 139: Simplified schematic of the variable gain amplifier (VGA) with dc bias voltages V_c, V_{b1} and V_b

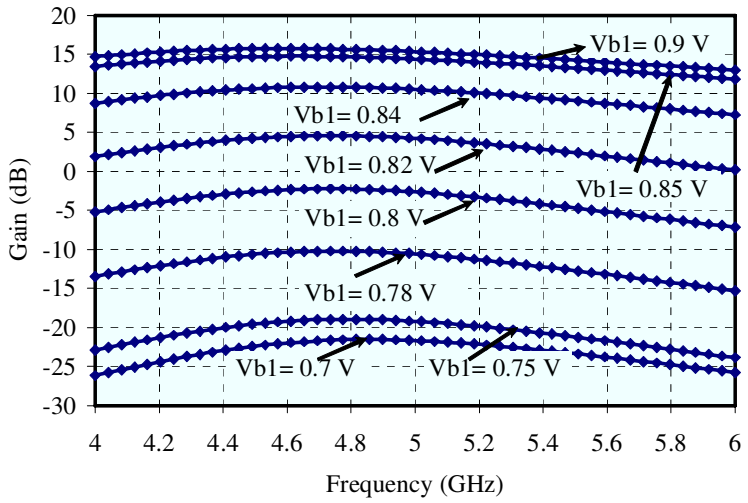


Figure 140: Simulated variation of gain versus frequency for different V_{b1} voltages of the cascode amplifier while keeping V_b = 2.36V and V_c = 3 V constant

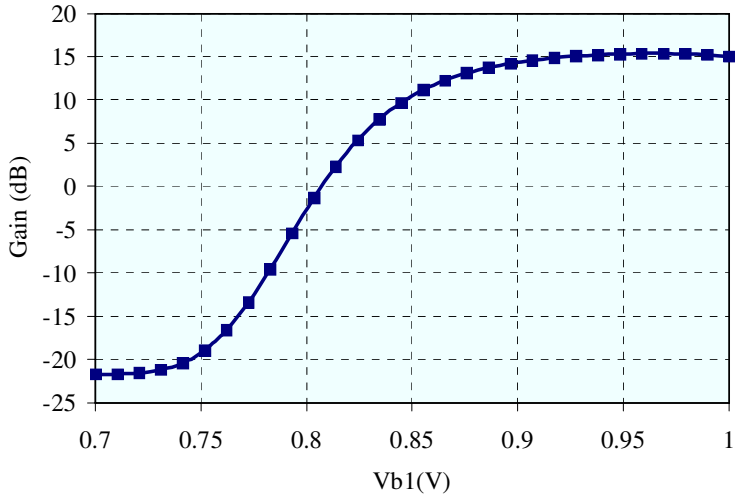


Figure 141: Simulated gain as a function of V_{b1} at 5 GHz while keeping V_b = 2.36V and V_c = 3 V constant

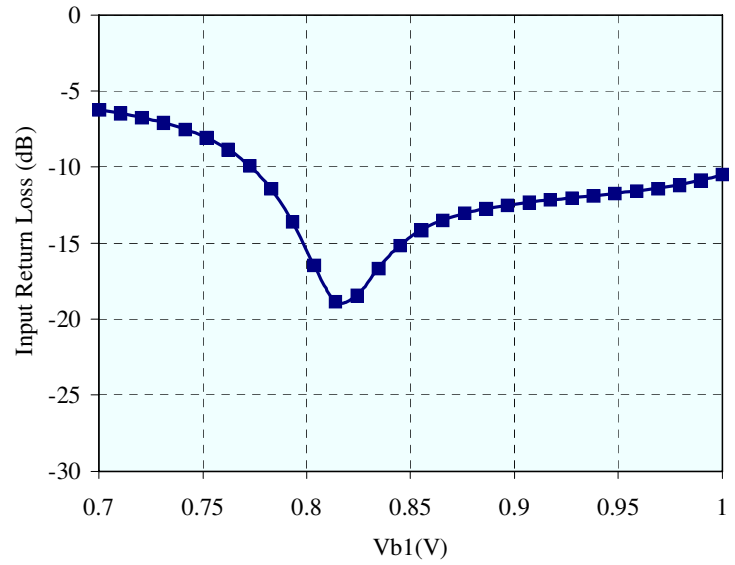


Figure 142: Simulated input return loss over the entire gain control range while keeping V_b=2.36V and V_c=3V constant

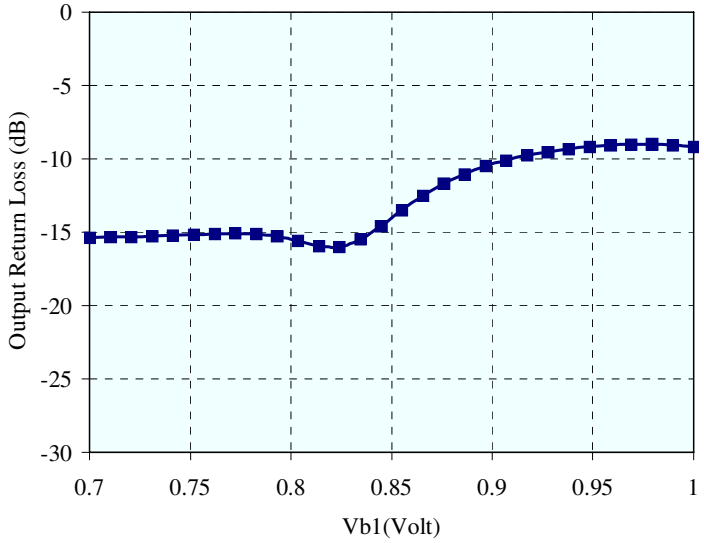


Figure 143: Simulated output return loss over the entire gain control range while keeping V_b = 2.36V and V_c = 3 V constant

Figure 144 shows the noise figure versus frequency at various voltage levels V_{b1} of the variable gain cascode amplifier. The noise is increasing since the decreasing V_{b1} moves the bias current away from the current for minimum noise. Figure 145 shows the simulated noise performance as a function of gain at 5 GHz. Over a gain-control range of 10 dB, the noise is increasing from 3 to 6.5 dB. The variation of noise figure is only 7 dB for a gain variation of 15 dB.

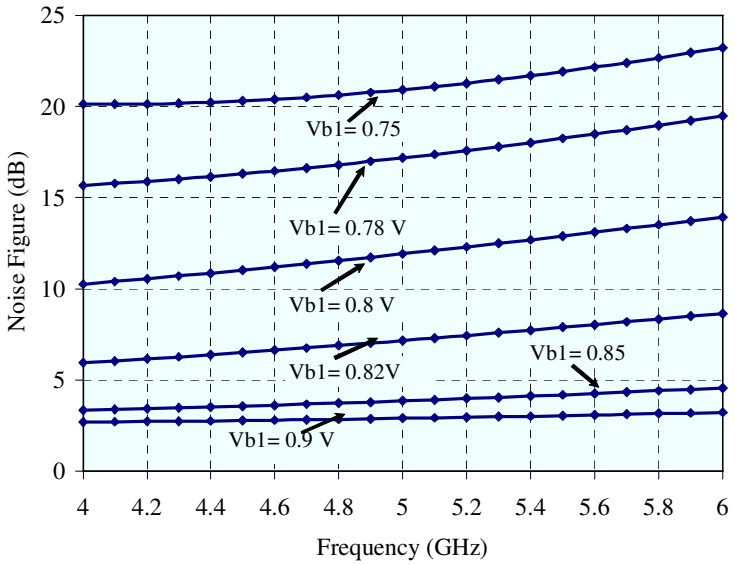


Figure 144: Simulated variation of noise figure versus frequency for different V_{b1} voltages of the cascode amplifier while keeping V_b = 2.36V and V_c = 3 V constant

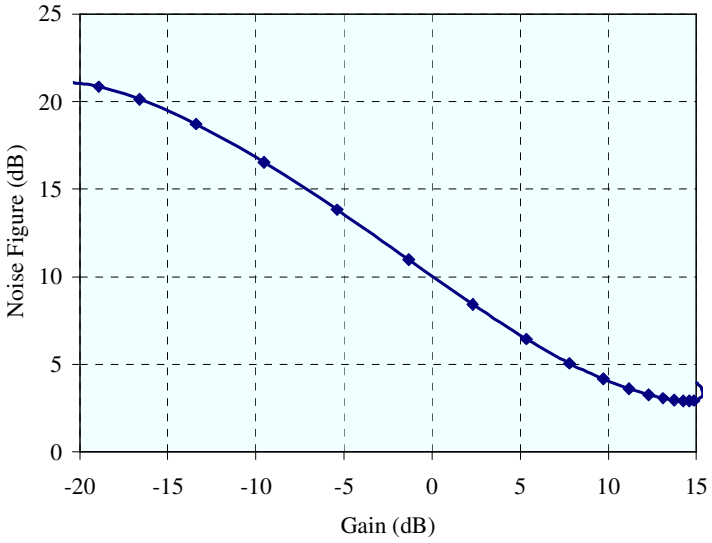


Figure 145: Simulated noise figure as a function of gain at 5 GHz while keeping V_b = 2.36V and V_c = 3 V constant

5.2.2.1.3 Hybrid 90° Coupler

The hybrid 90° coupler is a microwave circuit that is typically implemented using microstrip lines. It can also be implemented using lumped element equivalents, as shown in Figure 146. The component values are calculated as follows:

$$C_1 = \frac{1}{\omega_o Z_o},\ L_1 = \frac{Z_o}{\omega_o \sqrt{2}},\ C_2 = \frac{1}{\omega_o^2 L_1} - C_1 \tag{19}$$

where Z_0 is the input characteristic impedance and $_0$ is the center frequency. For a center frequency of $_0$ = 5.0 GHz, the lumped element values are C_1 = 0.637 pF, C_2 = 0.26 pF, and L_1= 1.13nH (after adjustments to compensate for parasitics). The simulated transmission magnitudes and phases for the coupler (including parasitics) are shown in Figure 147.

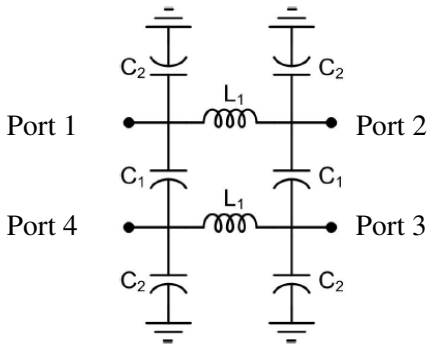


Figure 146: Simplified schematic of lumped element hybrid 90° coupler

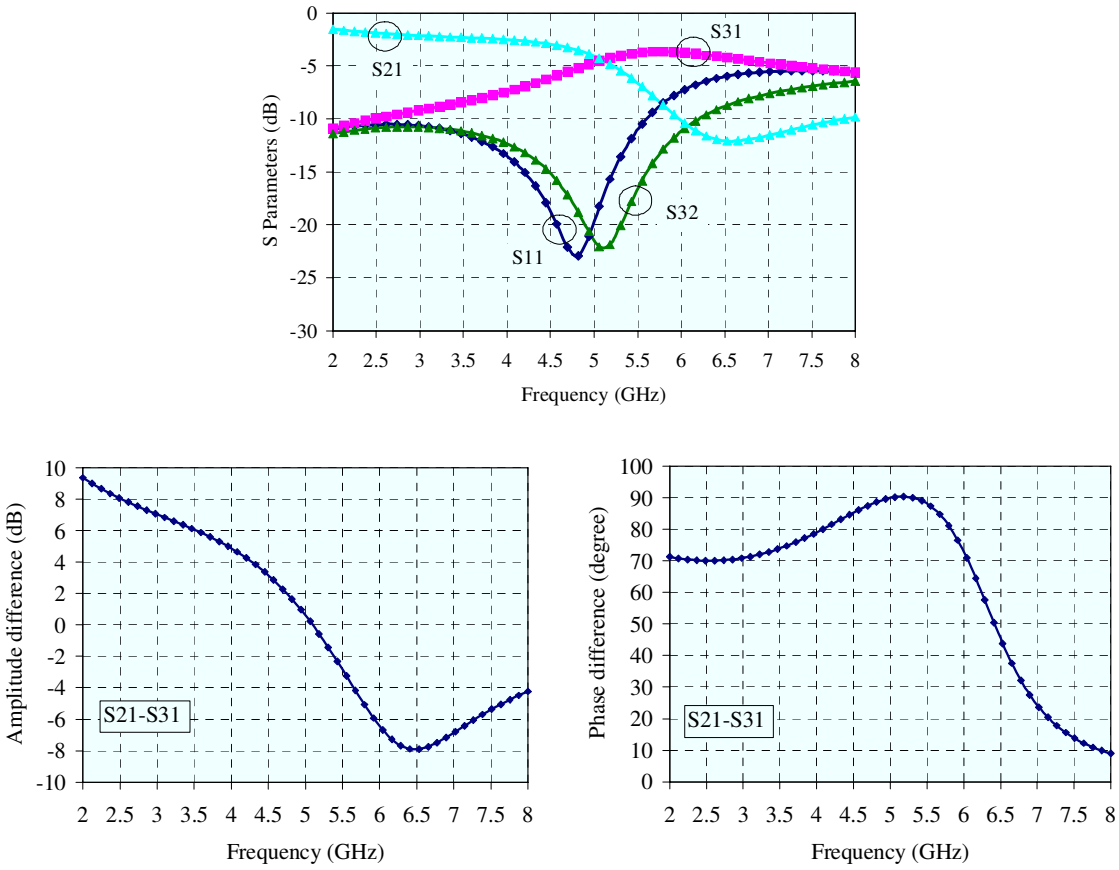


Figure 147: Simulated performance of a lumped element coupler built from foundry library elements (including parasitics)

Simulations using ADS were also used to determine the sensitivity of the coupler performance to variations in component values. It was found that a 10% change in the value of C_1 or L_1 resulted in a difference of 1.5 dB between the magnitudes of the two paths (S_{21} and S_{31}), with a negligible effect on the phase. Altering the value of C_2 by 10% had a negligible effect, and it was found that

removing the four C_2 capacitors only shifted the crossover frequency (the frequency where the incoming signal is evenly split) by 2.5%. The crossover frequency could then be restored to the desired value by reducing the size of the C_1 capacitors, resulting in an increase in loss of only 0.09 dB as compared to the coupler with the C_2 capacitors present, and the same relative phase shifts. This is likely because the calculated value for the C_2 capacitor is small compared to C_1, and the inductor has enough parasitic capacitance to ground to adequately perform the function of this capacitor. In designs where the omission of the C_2 capacitors will significantly reduce layout and wiring overhead, it may be a good choice to omit them, since the impact on performance is very small.

5.2.2.1.4 Lumped Wilkinson Power Divider

The quarter wavelength arms of a 5 GHz distributed Wilkinson divider are quite large. To make it more compact, a lumped element approach was used. Figure 148 shows the schematic and design parameters of a lumped Wilkinson power divider with a center frequency of 5 GHz. The lumped elements L and C are given by:

$$L = \frac{\sqrt{2}Z_o}{\omega_o} \text{ and } C = \frac{1}{\sqrt{2}\omega_o Z_o} \tag{20}$$

Figure 149 presents the simulated performance of a prototype using foundry models for the elements. The input return loss is better than 17 dB at the center frequency of 5 GHz. Simulated splitter losses from the input port to the two output ports are only about 0.7 to 1.2 dB higher than in the ideal case (3dB) for a frequency range of 4.5 to 5.5 GHz. Excellent isolation characteristics between the output ports, exceeding 25dB, are achieved.

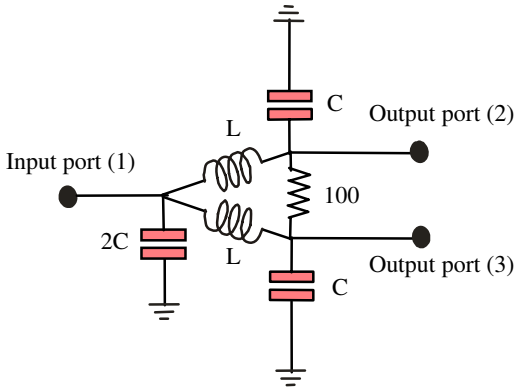


Figure 148: Simplified schematic of the lumped Wilkinson divider

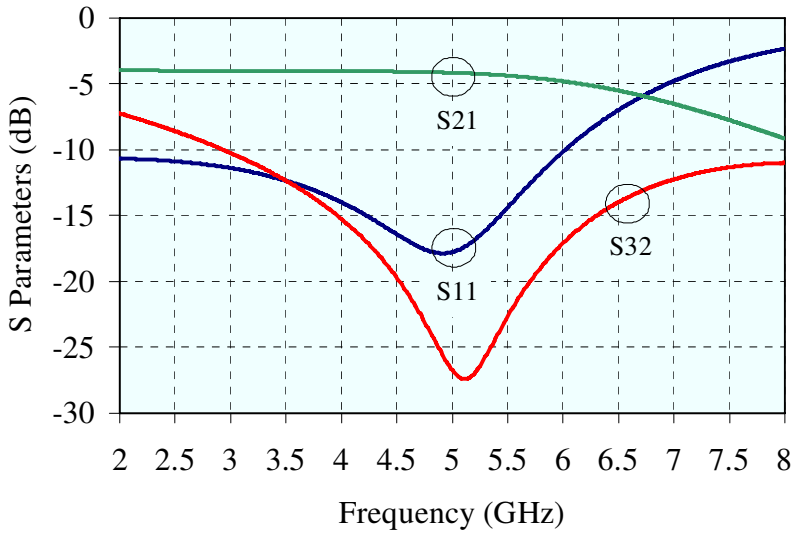


Figure 149: Simulated performance of a lumped element coupler built from foundry library elements (including parasitics)

5.2.2.1.5 Simulation Results of the 90° Vector Modulator Phase Shifter

The static constellation and frequency response of the 90º vector modulator phase shifter was simulated using Agilent ADS with sweep control voltages of 0.7 to 0.9 V for the two VGAs. Figure 150 shows the simulated magnitude and phase of the forward transmission coefficient in polar format for control voltages of two VGAs swept from 0.7 to 0.9 V. In the ideal case, the constellation should be in the first quadrant; however, from Figure 150 the phase shifter can still achieve 90° of phase shift and a S_{21} of 8 dB. Figure 151 shows the simulated small-signal gain corresponding to the various states at 5 GHz. The minimum loss at 5 GHz is around -27 dB, and the maximum gain is around 8 dB. The input and output return losses of the 90º vector modulator phase shifter at the various states are shown in Figure 152 and Figure 153, respectively. The input return loss is better than 10 dB, while the output return loss is better than 12 dB, at 5 GHz.

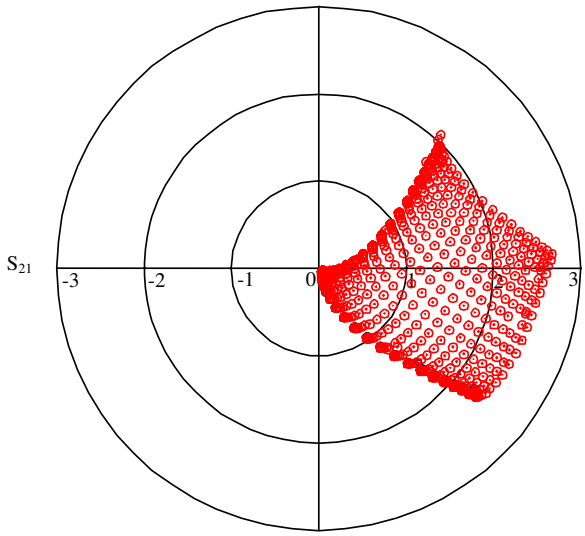


Figure 150: Simulated static constellation diagram of the 90º vector modulator phase shifter at 5 GHz with the control voltages of the two VGAs swept from 0.7 to 0.9V

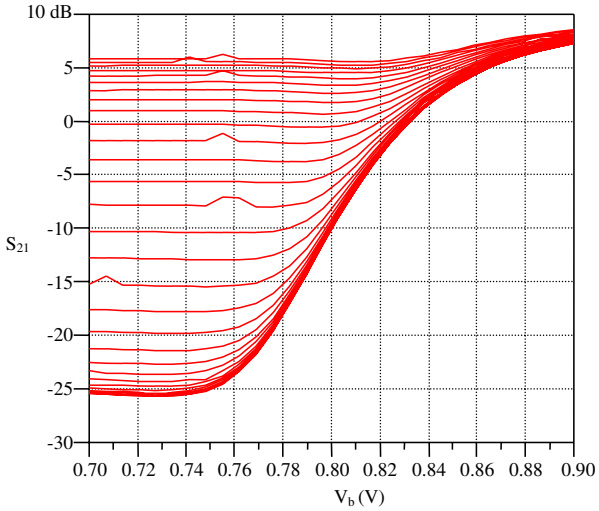


Figure 151: Simulated gain states of the 90º vector modulator phase shifter at 5 GHz

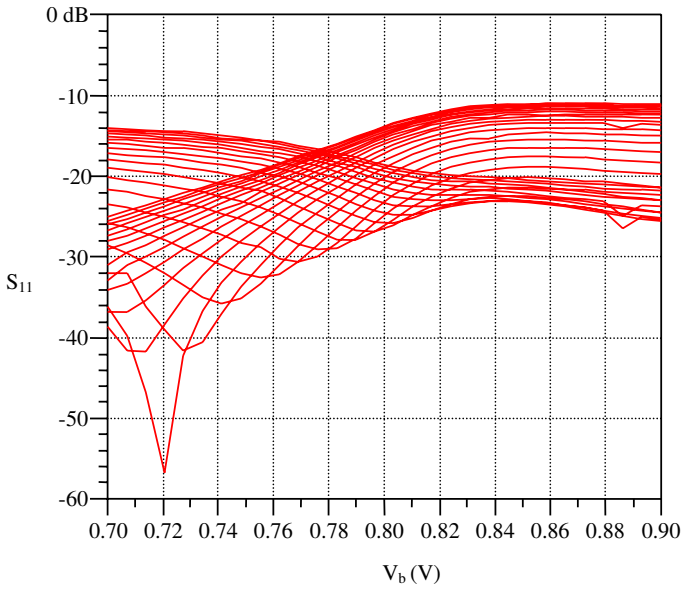


Figure 152: Simulated S_{11} of the various states of the 90º vector modulator phase shifter at 5 GHz

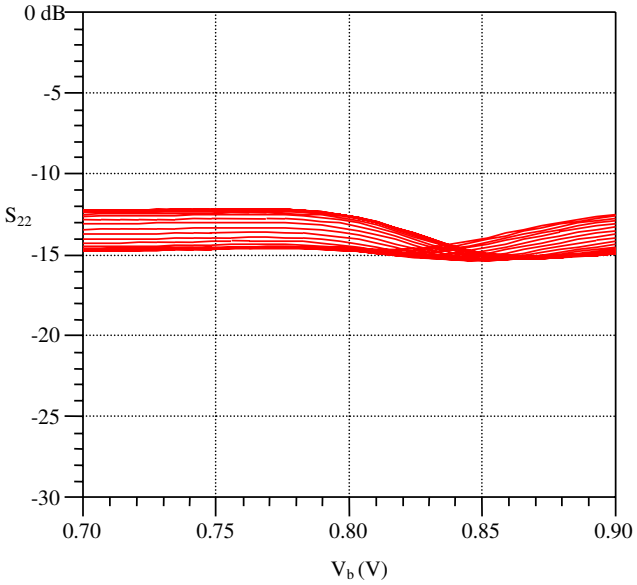


Figure 153: Simulated S_{22} of the various states of the 90º vector modulator phase shifter at 5 GHz

5.2.2.2 360° Vector Modulator Phase Shifter

Continuously variable phase shifters with a full 360° shift can be obtained by vector manipulation of four vectors with the vector angular separation being derived from mixers or quadrature couplers. Figure 154 illustrates the schematic of a continuously variable 0° to 360° phase shifter. The 360° phase shift is achieved by the sum of four quadrature vectors $A\angle 0°$, $B\angle 90°$, $C\angle 180°$, and $D\angle 270°$ with properly controlled amplitudes of A, B, C, and D.

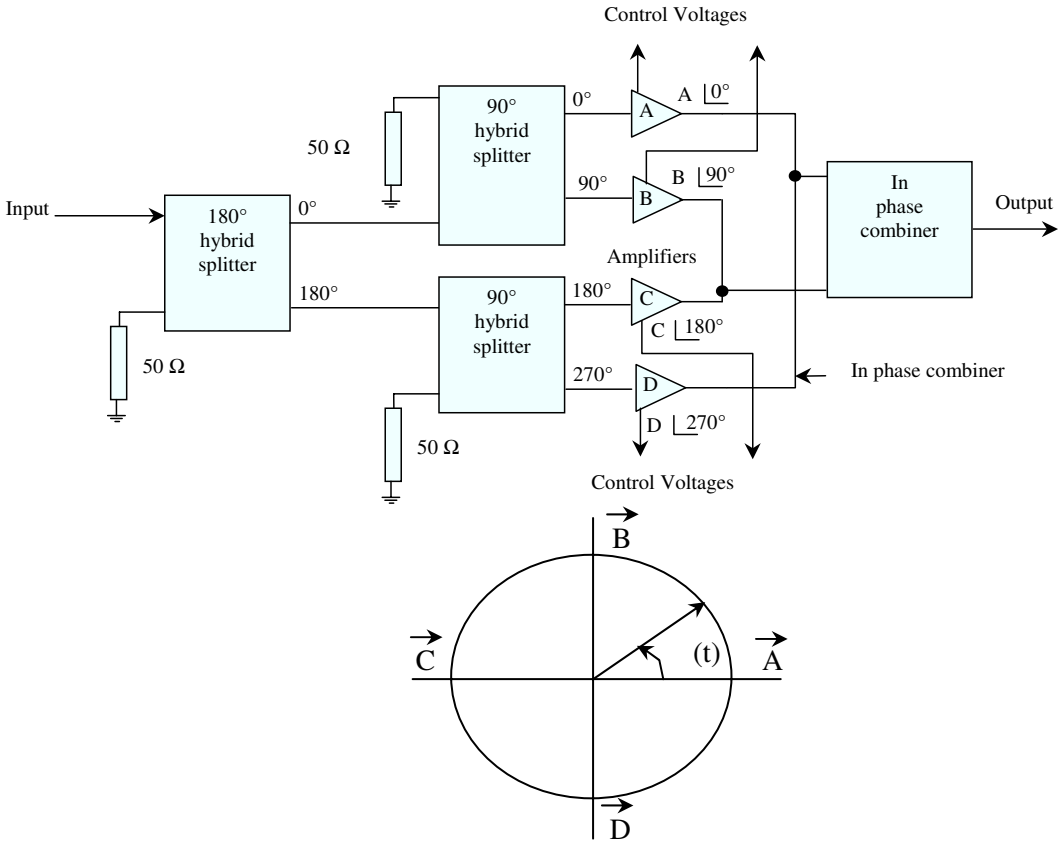


Figure 154: Schematic of a 360° vector phase shifter

These four quadrature vectors can be realized by a 180° power divider, two 90° hybrids, four cascode amplifiers and an in-phase, four-way power combiner as shown in Figure 154. The incoming signal is first divided into two signals, which are equal in amplitude but 180° apart in phase. Then each signal is further divided into two signals through 90° hybrids, resulting in four signals of equal amplitude and having phases of 0°, 90°, 180°, and 270°. Each signal is then amplified through cascode amplifiers, and the four outputs are then combined through cascaded 2-way in-phase combiners to obtain a phase-controlled output.

Figure 154 illustrates the four quadrants of the 360° phase shift, which are obtained using a combination of two vectors at a time. Each cascode amplifier serves as an amplifier-switch which can control the amplitudes of the vectors A, B, C, and D. As an example, when C and D are switched off, and A and B are switched on, an output signal with about 30° phase advance relative to the input signal is obtained (see Figure 154). By changing the second base bias voltages of amplifiers A and B (when C and D are switched off), 0° to 90° of phase shift can be obtained. Thus by controlling the bias voltages of two amplifiers at one time, while the other two are switched off, a total of 360° continuous phase shift can be obtained.

5.2.3 Reflective-Type Phase Shifter Analysis

The reflection-type phase shifter (RTPS) is a simple phase shifter design that uses a small number of components. It is most commonly an analog phase shifter with a single input control voltage. The RTPS can be realized in many different forms, but all include a quadrature hybrid coupler and dual, identical reflective loads as shown in Figure 155. The reflective loads are one-port circuits with variable phase reflection characteristics. The quadrature coupler's function is to isolate the input and output signals, turning the phase shifting behaviour of the reflective load into a more usable two-port device.

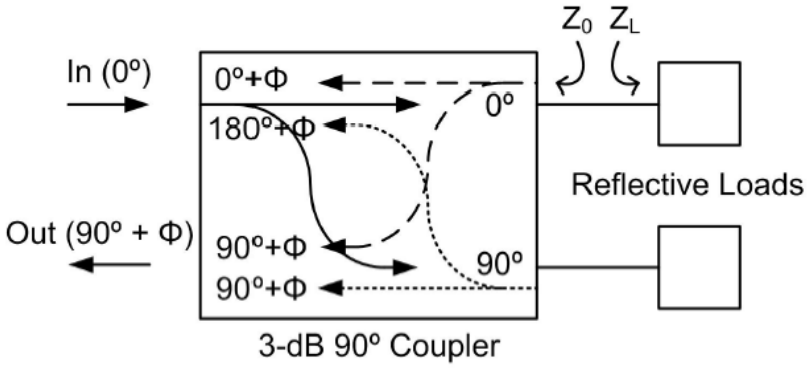


Figure 155: A reflective-type phase-shifter

The reflective load responsible for the phase shift can be realized in many different ways. The simplest is to use a tunable shunt capacitor. Realizing larger amounts of phase shift requires resonating the capacitor with an inductor or quarter-wave transmission line section. The most appropriate technique depends on the technology used to implement the phase shifter. Variables such as loss and size must also be taken into account when deciding on a reflective load topology.

The 90º hybrid coupler divides an input signal from any port into the two opposite ports, while isolating the adjacent one. In order to obtain the expected behaviour, two reflection loads must be included in the RTPS, connected to the coupled and thru ports of the hybrid. The RTPS's phase shifted input signal is found at the hybrid's isolated port, and will ideally be isolated from the RTPS input signal.

A RTPS uses a single control voltage, is relatively compact, and consumes no dc power.

5.2.3.1 Principle of the RTPS

A RTPS typically takes the form of a 3-dB hybrid coupler combined with two identical reflective loads. Its phase shift is determined by the phase angle of the reflection coefficient:

$$\Gamma = \frac{Z_R - Z_o}{Z_R + Z_o} \tag{21}$$

where Z_R is the impedance of the reflective load with minimum/maximum values of Z_{min} and Z_{max}, respectively, and Z_o is the characteristic impedance of the coupler. For a specific load reactance, X_R, the phase shift is:

$$\phi = -180 - 2\arctan\left(\frac{X_R}{Z_o}\right) \tag{22}$$

and the phase shift range is:

$$\Delta\phi = 2\left|\arctan\left(\frac{Z_{\max}}{Z_o}\right) - \arctan\left(\frac{Z_{\min}}{Z_o}\right)\right| \tag{23}$$

5.2.3.2 Reflective Load

The amount of phase shift that can be obtained from an RTPS is determined by the design of the reflective load. A number of common reflective loads are shown in Figure 156, the simplest of which is a single varactor (Figure 156(a)). The phase shift of the single varactor load can be increased by adding a series inductor, which resonates with the varactor at the operating frequency, adding a zero to the impedance function (single resonant load, Figure 156(b)). The phase shift can be further increased by adding a parallel capacitance, which adds a pole to the impedance function (transformed single resonant load, Figure 156(c)). Further increases in phase shift can be obtained by using two parallel single resonant loads, each resonating and introducing a zero at a different point in the varactor capacitance range (Figure 156(d)). The choice of reflective load depends on how much phase shift is required, the tuning range of the varactor, and the allowable loss. As the complexity of the reflective load increases, the total phase shift increases, as does the loss. For most silicon-based processes the passive components are of relatively low quality, so it is best to minimize the complexity of the load.

For this work we have chosen the transformed single resonated load (TSRL) in Figure 156(c). The analysis presented here assumes that the varactor has a capacitance tuning range of 2.5, which means that the maximum phase shift attainable with the TSRL is 360° although practical implementations will have less than this theoretical limit. Phase shifts of greater than 180° but less than 360º are adequate provided that differential signaling is used, since 360° of phase shift can be obtained by switching the polarity of the inputs to the phase shifter. The switching network necessary to obtain a full 360° range will introduce loss, so in a complete implementation the loss introduced by the switches would have to be compared with the loss introduced by using a more complex reflective load structure.

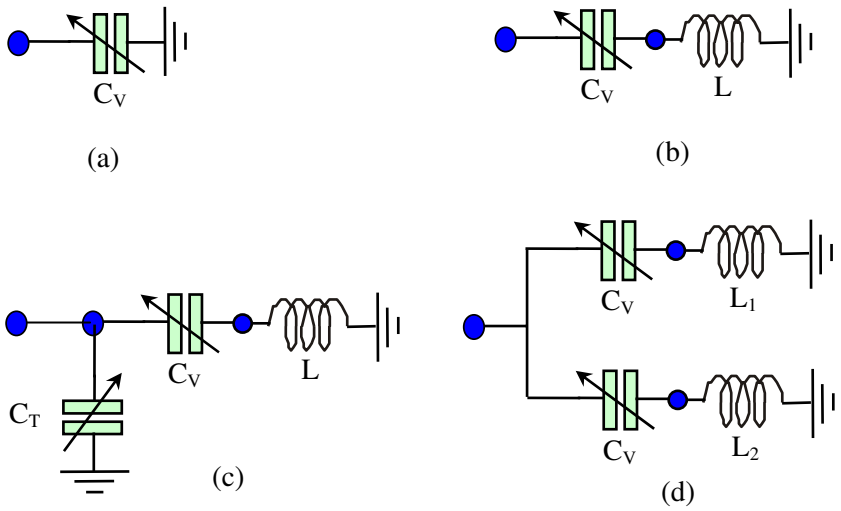


Figure 156: Reflective loads: (a) varactor, (b) single resonated load (SRL), (c) transformed single resonated load (TSRL), (d) dual resonated load (DRL)

5.2.3.2.1 Ideal Components

This section will analyze the TSRL assuming ideal components in order to size the components. The impedance of the circuit shown in Figure 156(c) can be expressed as

$$Z_L = \frac{1-\omega^2 LC_V}{j\omega\left(C_T + C_V - \omega^2 LC_T C_V\right)} \tag{24}$$

From (24) it can be seen that the TSRL impedance is purely imaginary (as expected), and assuming that is constant as C_V changes there are two singularities: one in the numerator where the TSRL impedance tends to zero and one in the denominator where the TSRL impedance tends to infinity. Designating the values of C_V where these singularities occur as C_N and C_D, respectively, then when the numerator is equal to 0:

$$1- \quad LC_N = 0 \tag{25}$$

and when the denominator is equal to 0:

$$C_T+C_V- \quad LC_V\, C_T = 0 \qquad C_T + C_D - C_D C_T/C_N = 0 \qquad C_T\,(C_N-C_D) + C_D\, C_N = 0 \tag{26}$$

Equations (25) and (26) can be rearranged to become $L = 1/\ ^2C_N$ and $C_T = C_D C_N/(C_D - C_N)$ which in turn can be used to express (24) as:

$$Z_L = \frac{1 - {}^{C_V}\!/_{C_N}}{j\omega C_T (1 - {}^{C_V}\!/_{C_D})} \tag{27}$$

Since the change in the phase shift is determined by the change in the impedance, the greatest change in the phase shift will occur when C_V is in the range of C_D, since the impedance will transition from a finite value to infinity to negative infinity and back to a finite value. This is shown in Figure 157 where the phase shift and impedance are plotted against C_V. In this and the following plots we have assumed an operating frequency of 5 GHz and a tuning range of 2.5. From Figure 157 it can be seen that the phase changes most rapidly around C_D, which has been set to the middle (arithmetic mean) of the tuning range. From this we can conclude that a good choice for C_D is in the middle of the tuning range.

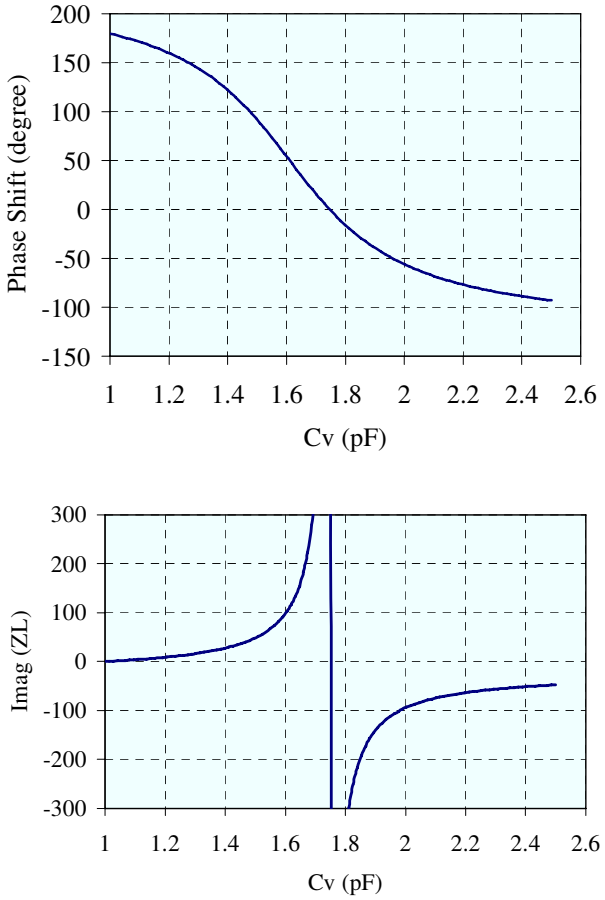


Figure 157: RTPS phase shift superimposed on TSRL impedance over the varactor range

The rate of change of the phase will be determined by the rate of change of the impedance, and this is set by the proximity of C_N to C_D, as well as by the magnitude of C_V. We have assumed that C_D is chosen at the middle of the tuning range, and C_N is chosen to be less than C_D. As C_N moves closer to C_D, the impedance changes more quickly in the neighborhood of C_D, and thus the slope

of the phase shift increases. This is plotted in Figure 158, where the phase shift is plotted for C_N increasing from $C_{V,min}$ to $1.5C_{V,min}$. As C_N decreases the slope increases and the total phase shift approaches the limit of 360° (for a varactor tuning range of 2.4).

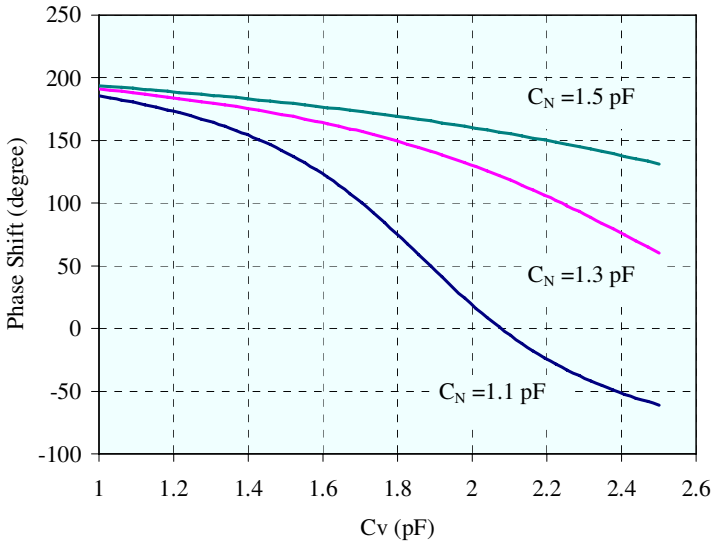


Figure 158: Effect of zero location (value of C_N) on phase shift characteristics

The range of phase shifts as a function of C_N is plotted in Figure 159. Increasing the nominal value of C_V has a similar effect to moving C_N closer to C_D. From these plots we can see that the choice of C_N is a compromise between the phase shift range and the slope of the phase shift curve. For higher slopes the phase shift will be more sensitive to noise on the control voltage of the varactor. In the presence of non-ideal components, the higher slope in the phase shift curve also leads to higher losses.

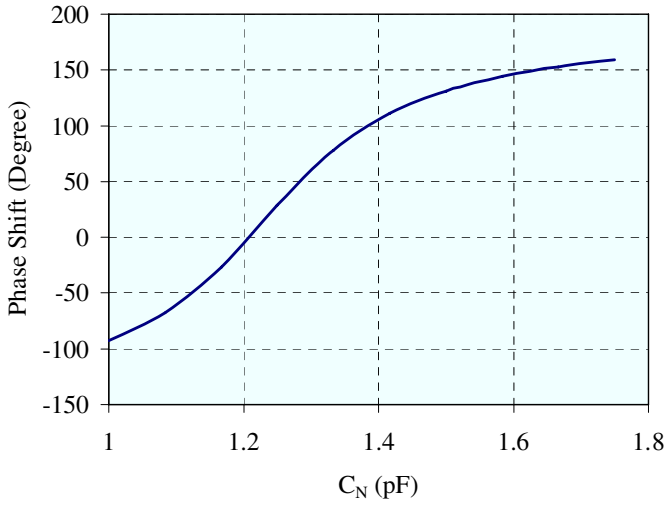


Figure 159: Phase shift range vs. zero location (value of C_N)

5.2.3.2.2 Impact of Parasitics

This section will analyze the first-order effects of parasitics on the phase shift characteristics. The circuit that will be analyzed is shown in Figure 160. The circuit includes a series resistance, R_p, that results from the parasitic resistance in the varactor or the inductor (or both).

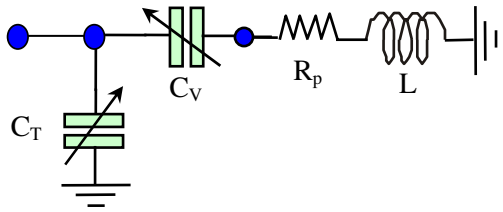


Figure 160: TSRL including parasitic series resistance

The impedance of the circuit shown in Figure 160 can be expressed as:

$$Z_L = \frac{1 - \omega^2 LC_V + j\omega R_P C_V}{j\omega(C_T + C_V - \omega^2 LC_T C_V) - \omega^2 R_P C_T C_V} \tag{28}$$

Comparing (24) with (28), we can see that the parasitic resistor has created an additional term in both the numerator and denominator. As expected, as R_P 0, the last terms in the numerator and denominator of (28) disappear, and it becomes identical to (24). We can also observe that as C_V and C_T become smaller, the extra terms created by R_P will be less significant, and the behavior will more closely approximate the ideal case.

To see the effect of the parasitic resistance on the phase shift, we can plot the phase shift for increasing values of R_P. This is shown in Figure 161 for $C_{V,min}$ of 1 pF and R_P values from 0 to 8Ω. It can be seen that as R_P increases, the slope of the phase shift in the vicinity of $C_V = C_N$ increases. For $R_P > 4.5\Omega$ the phase shift characteristics change completely; the phase shift is greatly reduced and is no longer monotonic. Also, larger values of C_V greatly decrease the tunability of the phase shifter. For example, $C_{V,min}$ = 1 pF the phase shifter switches to non-monotonic behavior at $R_P = 4.73\Omega$, while for $C_{V,min}$ = 10 pF (and C_N chosen to provide similar slope in the phase shift characteristics) the phase shifter switches to non-monotonic behavior at a much smaller R_P of 0.41Ω. The additional term in the denominator is also proportional to C_T, so we can observe that the sensitivity to R_P will increase as C_N moves closer to C_D (which increases the phase shift by steepening the phase shift characteristics in the vicinity of C_D). From this analysis, it is evident that the value of the varactor in the TSRL should be chosen as small as is practical to minimize sensitivity to parasitic resistance.

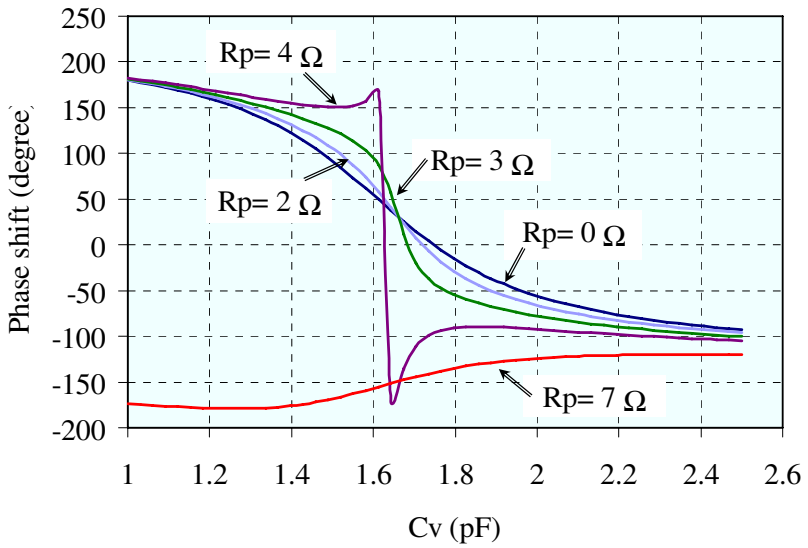


Figure 161: Effect of parasitic series resistance on phase shift

5.2.3.3 Design Strategy

This section will consolidate the findings of the previous sections into a general procedure to design a RTPS with a TSRL. The initial design should be simulated using ideal components, then simulated with models that include component parasitics, and finally simulated with extracted models which include layout parasitics, with adjustments to component values being made at each step as necessary. These steps are shown in Figure 162.

Following the last step in Figure 162, component models should be introduced for the varactor, capacitor, and inductor. After doing this, the greatest effect on the phase shift characteristics will be due to the parasitic resistances in the non-ideal components. If after re-simulating the circuit the phase shift is greatly reduced and non-monotonic it will be necessary to return to the first step and redo the sizing procedure with a larger value of L (and thus a smaller C_V) to reduce the sensitivity to the parasitic resistance. The loss of the RTPS should also be simulated at this point and the loss will be greatest in the vicinity of C_D. If the loss is too large, it can be reduced by moving C_N away from C_D and reducing the slope of the phase shift characteristics.

Finally, extract and simulate the circuit from the layout. The largest effect on the phase shift characteristics after this step will be due to the parasitic capacitance to ground. This can be compensated for by adjusting C_N and C_D and re-calculating C_T to restore the pole and zero to their desired locations, and by adjusting the varactor range if necessary.

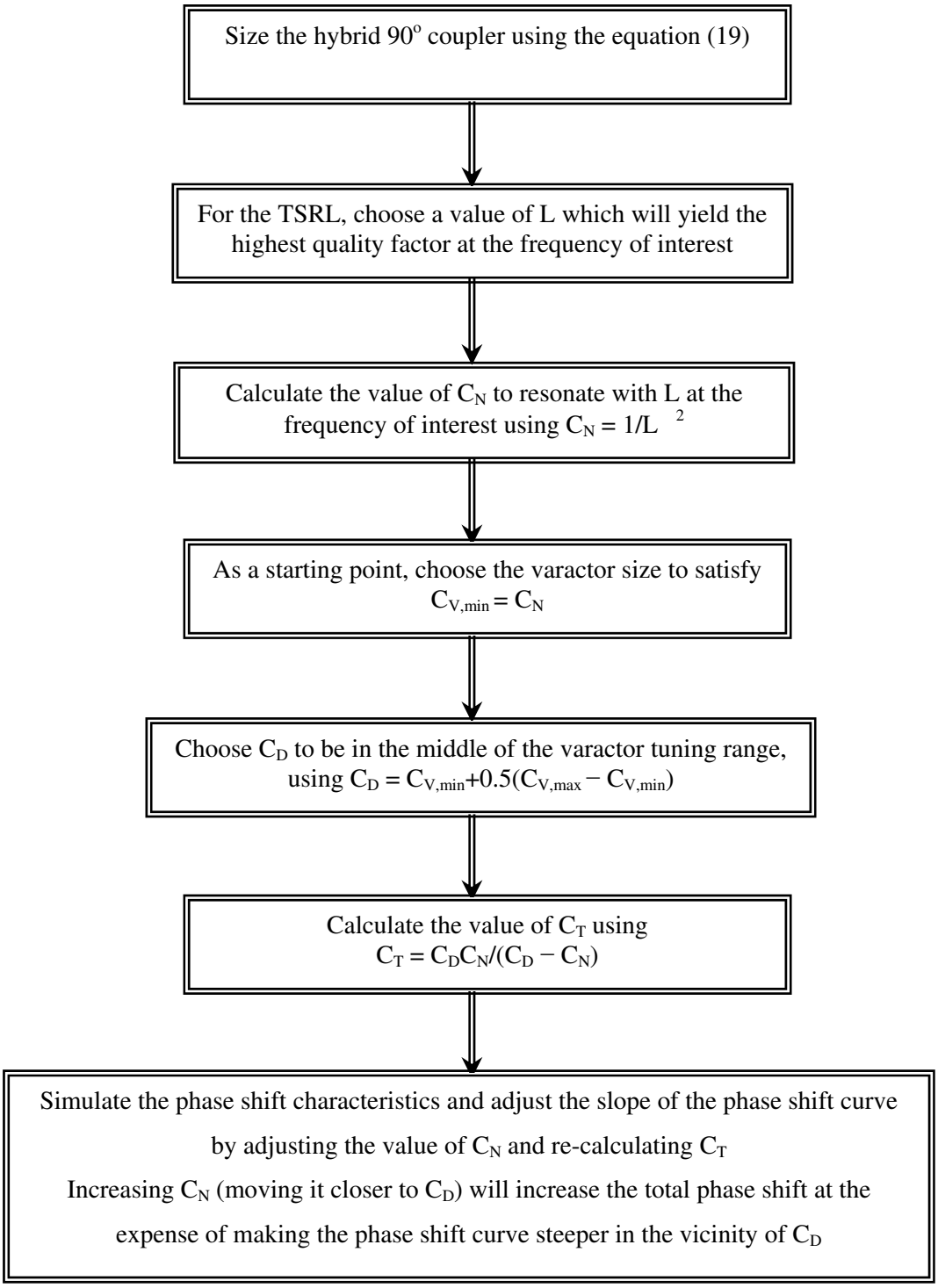


Figure 162: RTPS design strategy

5.2.3.4 Reflective-Type Phase Shifter (RTPS) Design

In this section we will report the performance of the RTPS that was designed using the methods and analysis outlined above. The hybrid 90° coupler is shown in Figure 163 and was designed using (19) for f_0 = 5 GHz. The schematic of the TSRL is also shown in Figure 163. Capacitors C_{B1} and C_{B2} are blocking capacitors to allow proper biasing of the varactors. The component values were chosen using the design procedure outlined in the previous section, and then adjusted after simulations to minimize loss and maximize the phase shift range. Blocking capacitor C_{B1} was sized considerably smaller than the other blocking capacitors in order to minimize the parasitic capacitance to ground that is introduced between the bottom plate and the substrate. Resistor R_{bias} is used to bias the varactors and is effectively in parallel with the varactor so it should be sized large to maintain a high quality factor, but small enough to avoid degrading the noise figure. For this work, R_{bias} was sized at 5 k and implemented on chip with a P^+ polysilicon resistor. The varactor was implemented with a SiGe varactor, with a tuning range of t = 2.23.

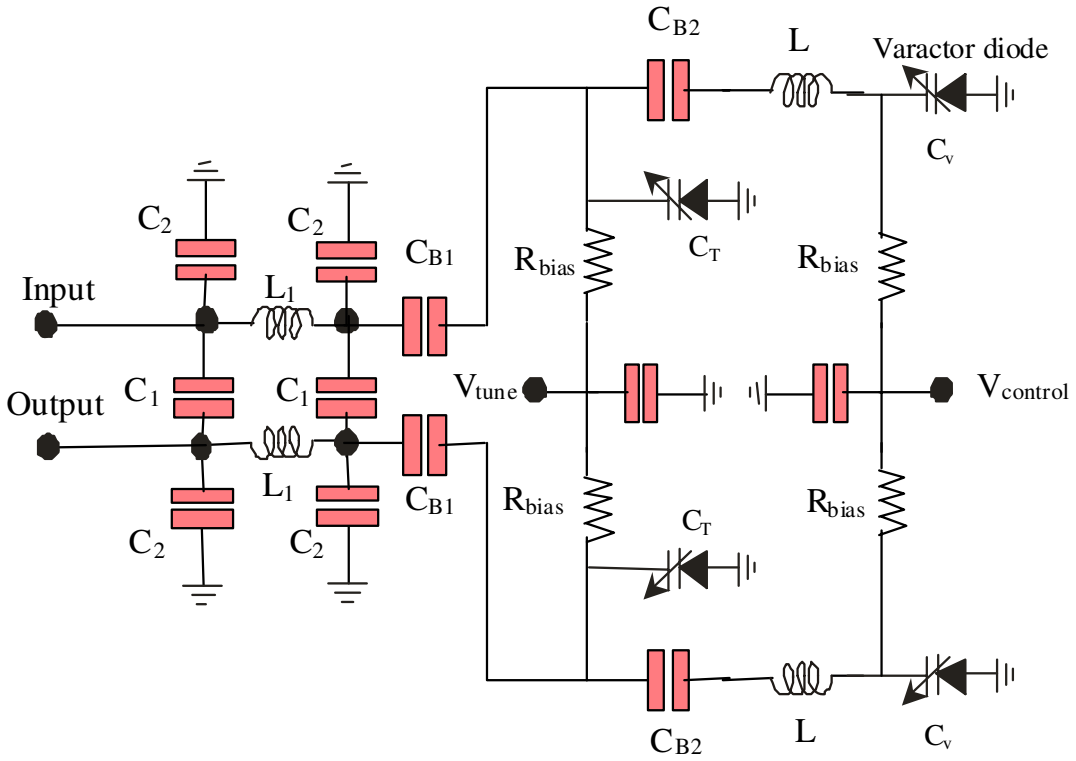


Figure 163: Circuit topology of the RTPS with TSRL loads

Figure 164 to Figure 166 show the simulated relative phase shift, insertion loss, and return loss of the phase shifter at 5 GHz with respect to the varactor control voltage, $V_{control}$. The simulated maximum relative phase shift is 240° over the 0 – 3V control range. The simulated loss over the nominal phase shift range is shown in Figure 165, and it can be seen that the loss varies from -10 dB to -40 dB. Unfortunately this configuration results in large loss variations. For the circuit, the return loss is better than 18 dB. One of the inherent advantages with this RTPS is its excellent return loss performance. This enables the RTPS to be embedded between two high gain

amplifiers, required to overcome the high levels of insertion loss, without increasing the risk of instability.

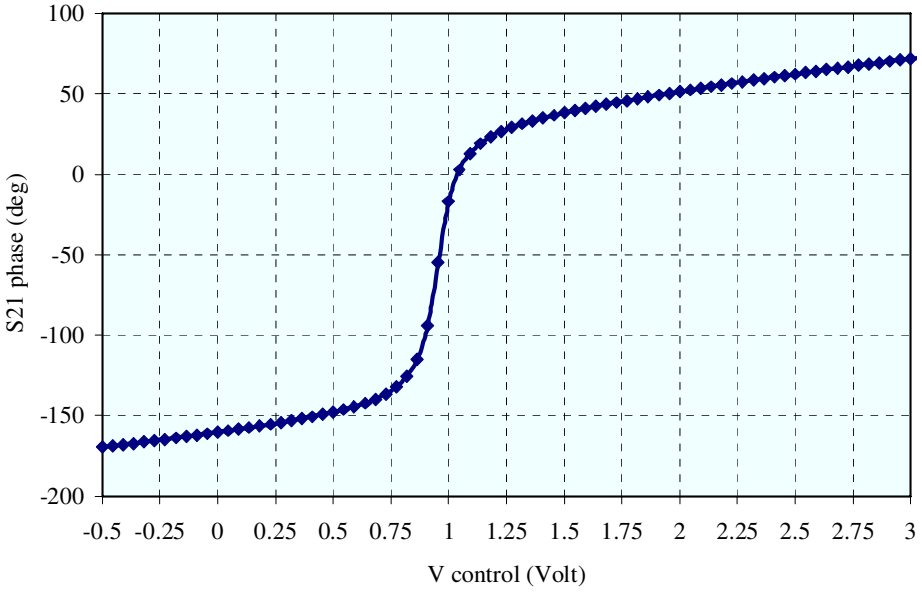


Figure 164: Simulated phase shift of the RTPS

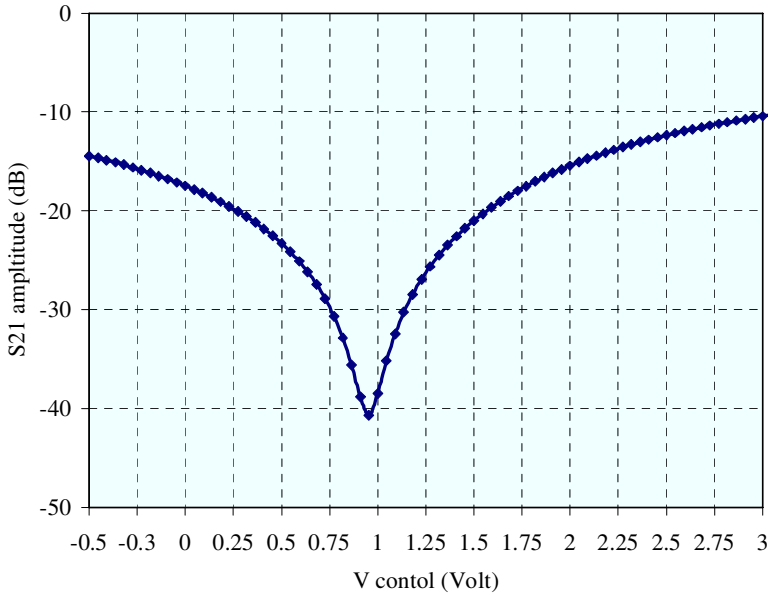


Figure 165: Simulated insertion loss of the RTPS

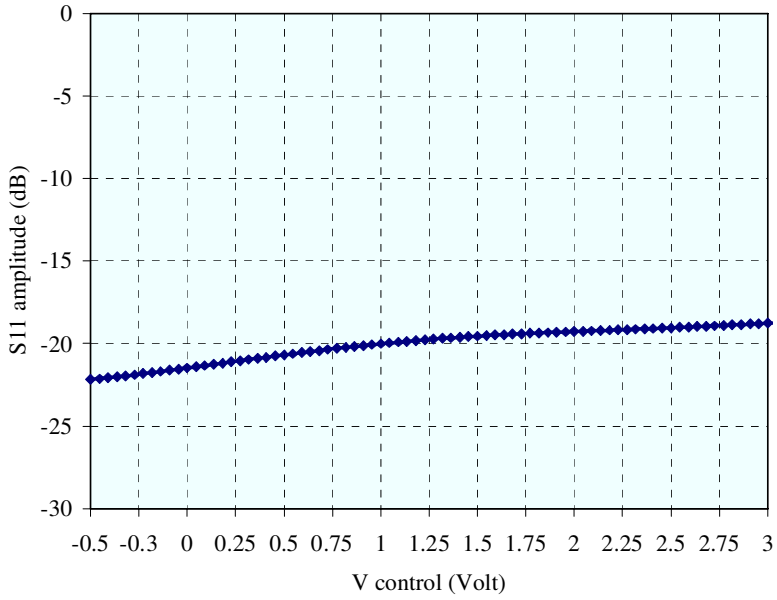


Figure 166: Simulated return loss of the RTPS

The frequency limitation of this phase shifter is mainly from the coupler itself. Figure 167 shows the simulated phase shift of the circuit from 4 to 5 GHz. The simulated maximum relative phase shift range is larger than 200°.

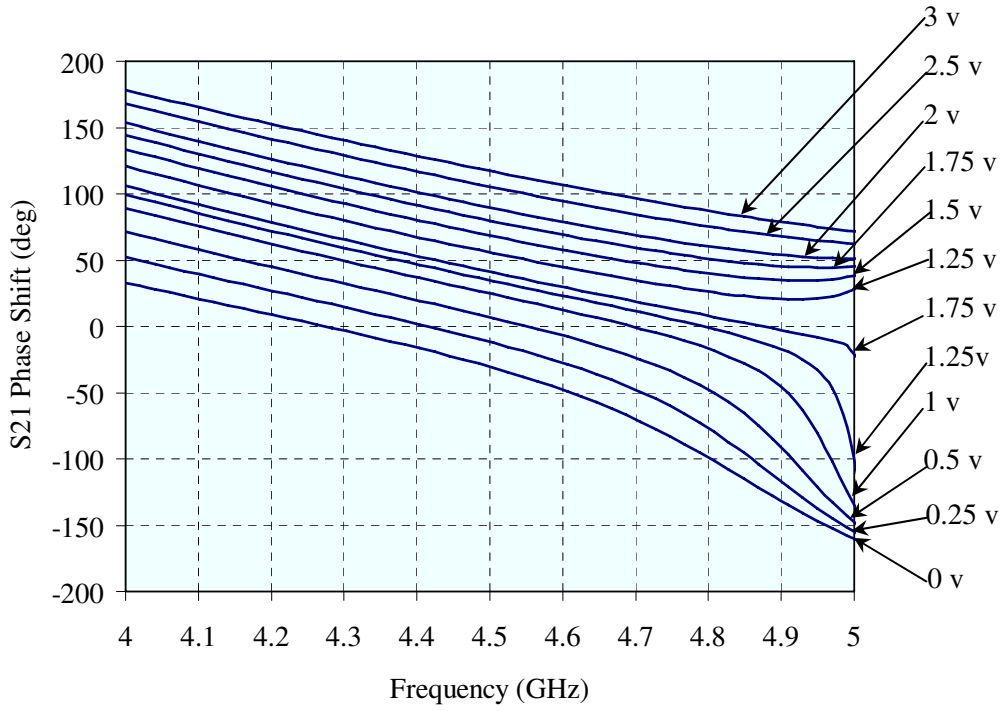


Figure 167: Simulated S_{21} performance versus frequency and control voltage $V_{control}$

5.2.4 Experimental Results

5.2.4.1 Variable Gain Amplifier Measurements

The variable gain amplifier was designed with a 0.35 m SiGe HBT process as outlined in Section 5.2.2.1.2. For small signal measurements, the VGA chips were mounted on a probe station with RF connections made by 150-µm pitch coplanar probes and DC biasing applied through a ground-power-power-ground (GPPG) probe. The results were measured with a vector network analyzer connected to a single ended output 50 port. The collector and base bias voltages (V_C, V_b) of the common base stage are 3V and 2V respectively, and the control voltage V_{b1} of the common emitter can vary from 0.7 to 1 V.

Figure 168 to Figure 170 show the measured gain control range and input/output return loss characteristics of the VGAs as a function of control voltage, V_{b1}, at 5 GHz. A dynamic gain control range of 45 dB is achieved by adjusting V_{b1} over a range of 0.7 to 1 V. A maximum gain of greater than 10 dB is obtained at V_{b1}= 0.9V. Figure 171 shows the wideband variable gain response from 4 GHz to 6 GHz at various control voltages V_{b1}. The plot illustrates over 45 dB of gain control. The gain flatness is less than 2 dB over the full 4-6 GHz frequency band and 45 dB gain control range.

At 5 GHz, the input return loss illustrated in Figure 172 is better than 10 dB over the range of control voltages V_{b1}. The variation in output return loss, shown in Figure 173, is less than 3dB over the control voltage range at 5 GHz.

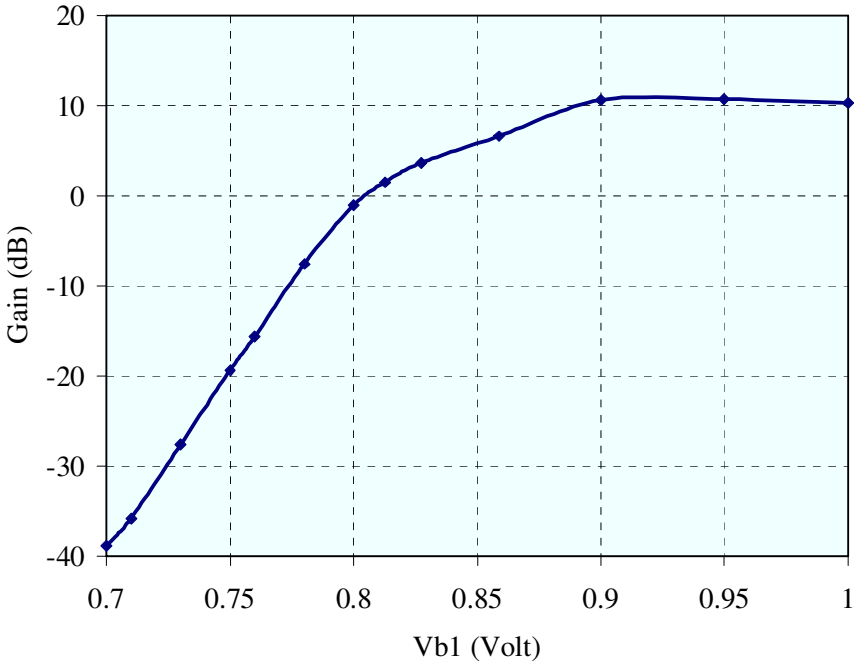


Figure 168: Gain as a function of V_{b1} at 5 GHz

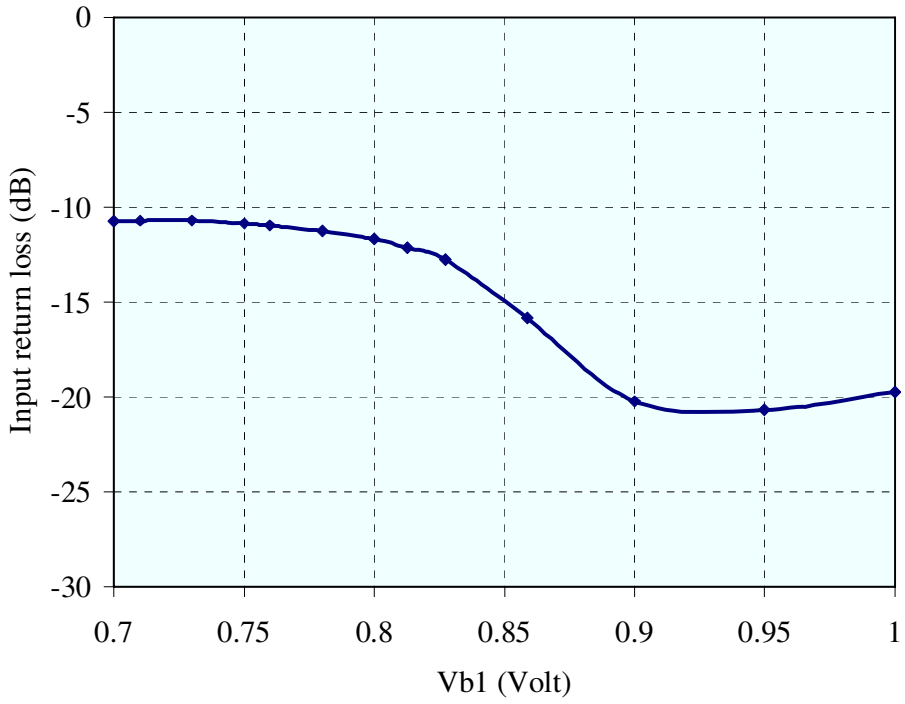


Figure 169: Input return loss over the entire gain control range

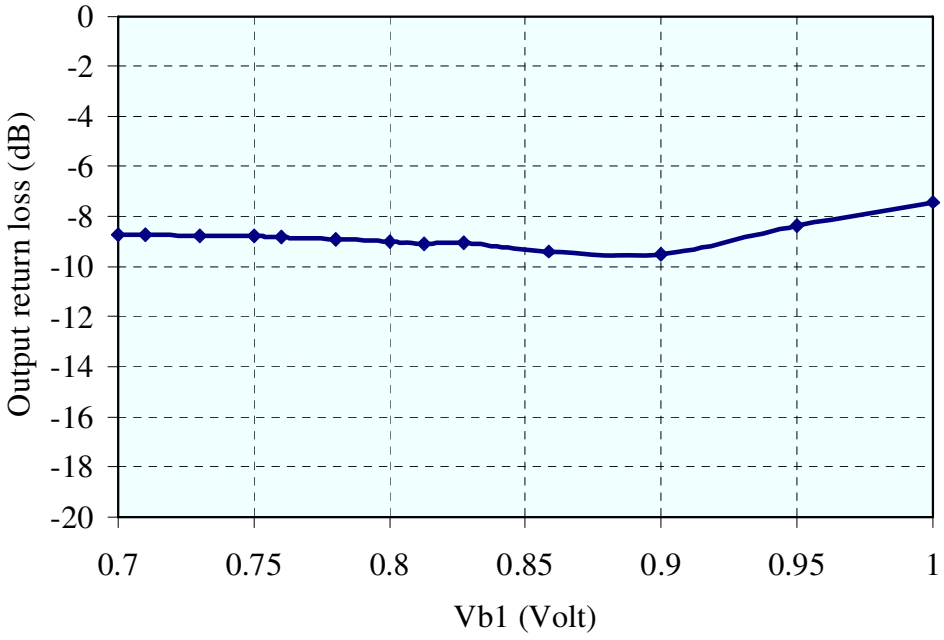


Figure 170: Output return loss over the entire gain control range

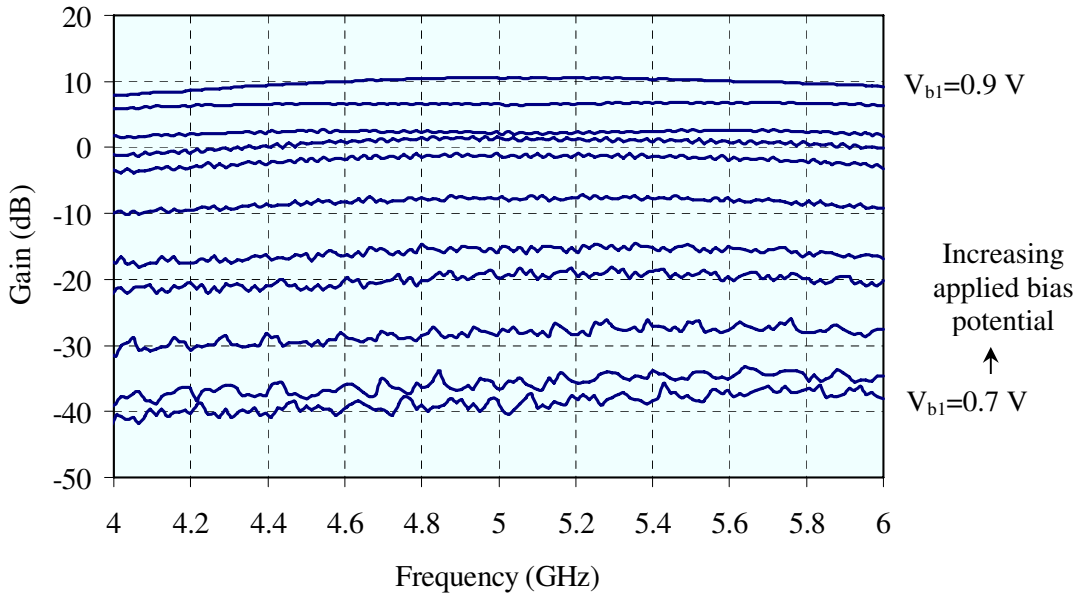


Figure 171: Variation of the gain versus frequency for different V_{b1} voltages of cascode amplifier while keeping V_b = 2 V and V_c = 3 V constant

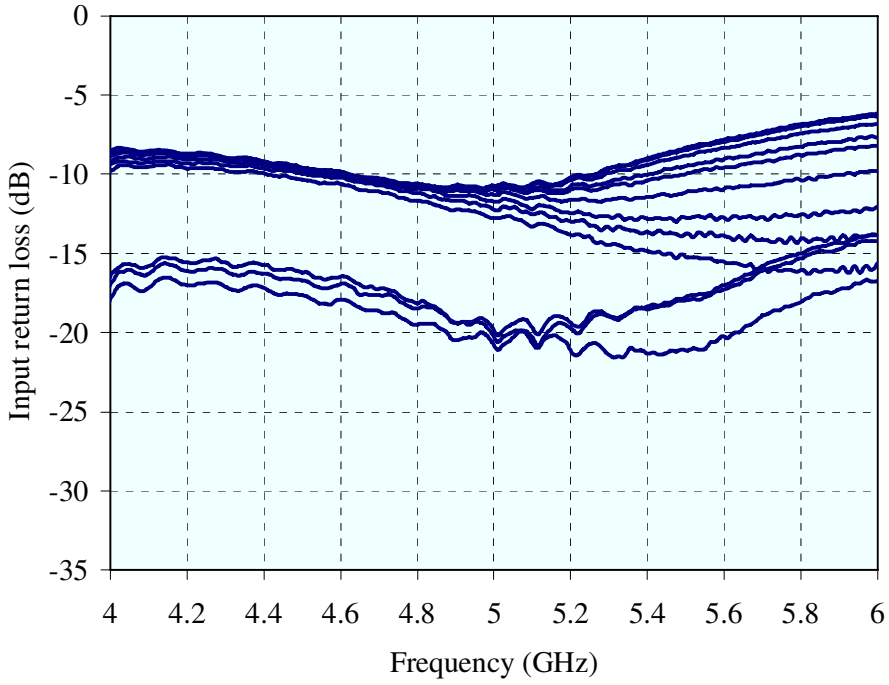


Figure 172: Variation of input return loss versus frequency for different V_{b1} voltages

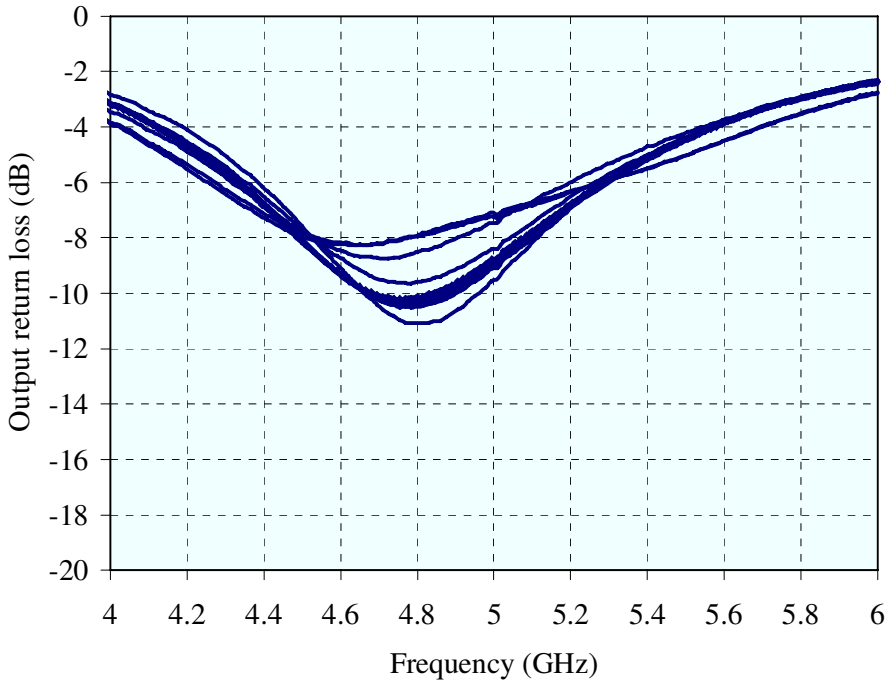


Figure 173: Variation of output return loss versus frequency for different V_{b1} voltages

5.2.4.2 90° Vector Modulator Phase Shifter Measurements

The 90º vector modulator phase shifter was fabricated using a 0.35 m SiGe HBT process. The chip photograph of the total phase shifter is shown in Figure 174.

Figure 175 shows the measured small-signal gain corresponding to various states from 3 to 6GHz. An Agilent N6705A DC Power Analyzer is used to control the bias of the VGAs to realize the various states. Specifically, the control voltages of the two VGAs (the common-emitter base bias voltages) were swept from 0.7 to 1 V in steps of 0.014 V. The minimum S_{21} is about -43 dB at 5GHz whereas the maximum is around 6.8 dB.

The return losses of the 90º vector modulator phase shifter at various states are shown in Figure 176 and Figure 177. The worst-case input return loss is 8 dB over the entire range from 3 to 6 GHz, and the worst-case output return loss is 10 dB from 4.5 to 6 GHz for all states.

A static constellation diagram was obtained from a continuous-wave (CW) mode parameter measurement using the N6705A DC Power Analyzer. The forward transmission coefficients S_{21} for the states are plotted in Figure 178 in polar format. The control voltages of two VGAs have been swept from 0.7 to 1 V in steps of 0.014 V. The ideal S_{21} of the 90º vector modulator phase shifter should look like a square in the first (upper-right) quadrant with the center should be the origin point of the polar chart in Figure 178. However, from Figure 178, continuous polar modulation with a 50-dB dynamic range can still be achieved with a maximum S_{21} of 6.8 dB.

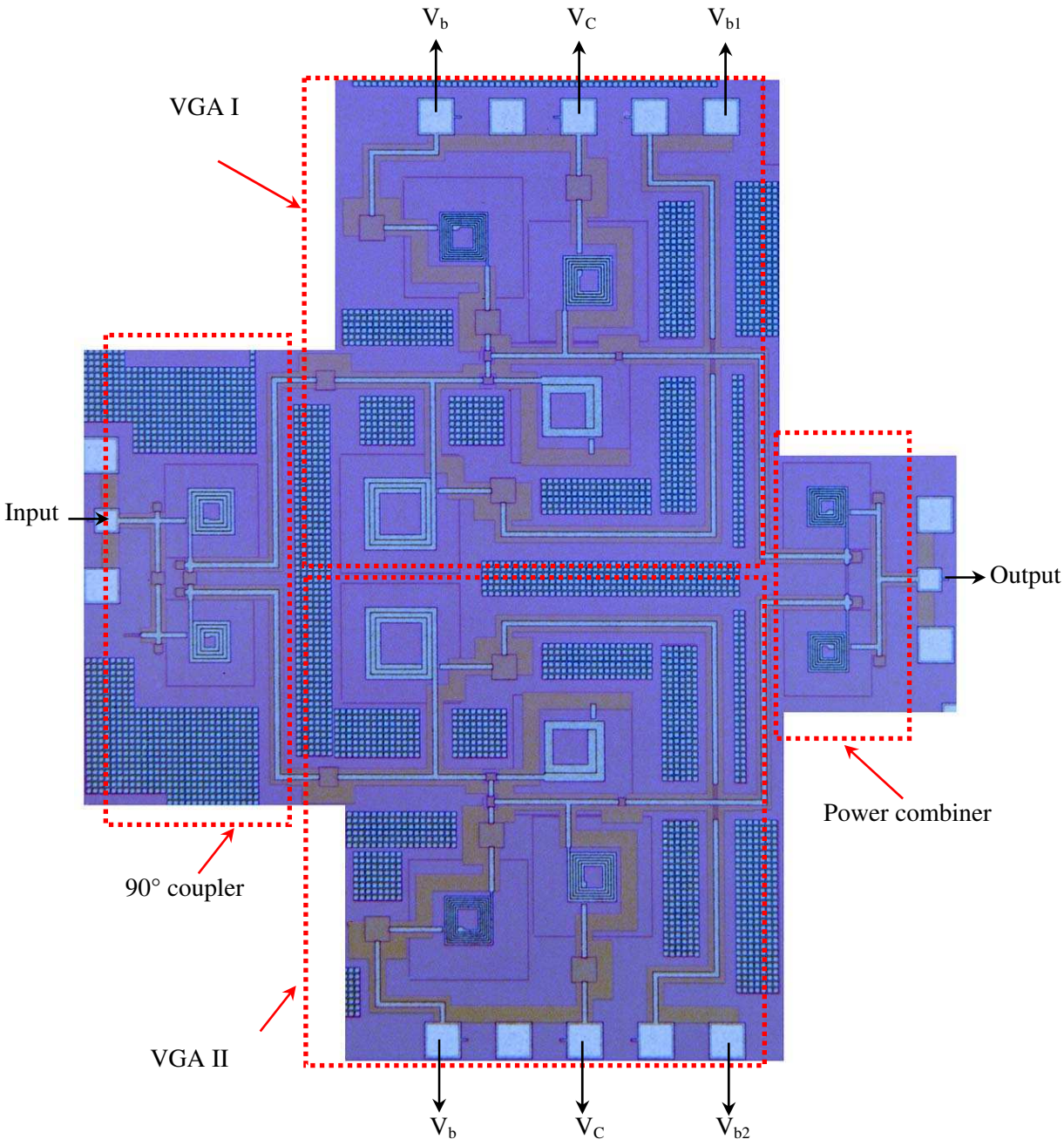


Figure 174: Chip photograph of the 90º vector modulator phase shifter

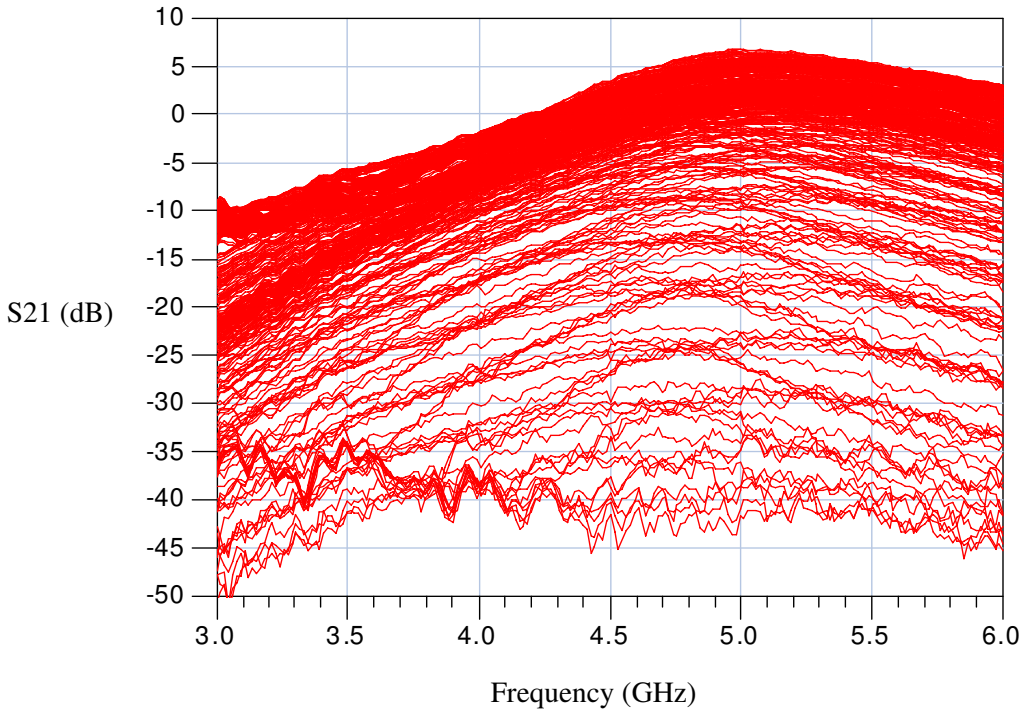


Figure 175: Measured gain of the 90º vector modulator phase shifter at various states

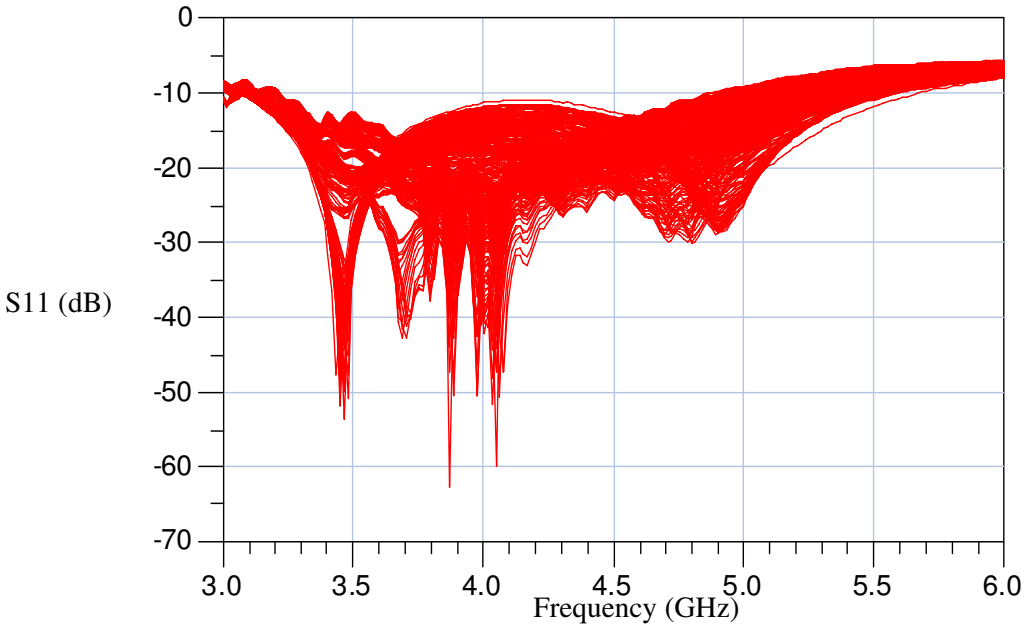


Figure 176: Measured input return loss of the 90º vector modulator phase shifter at various states

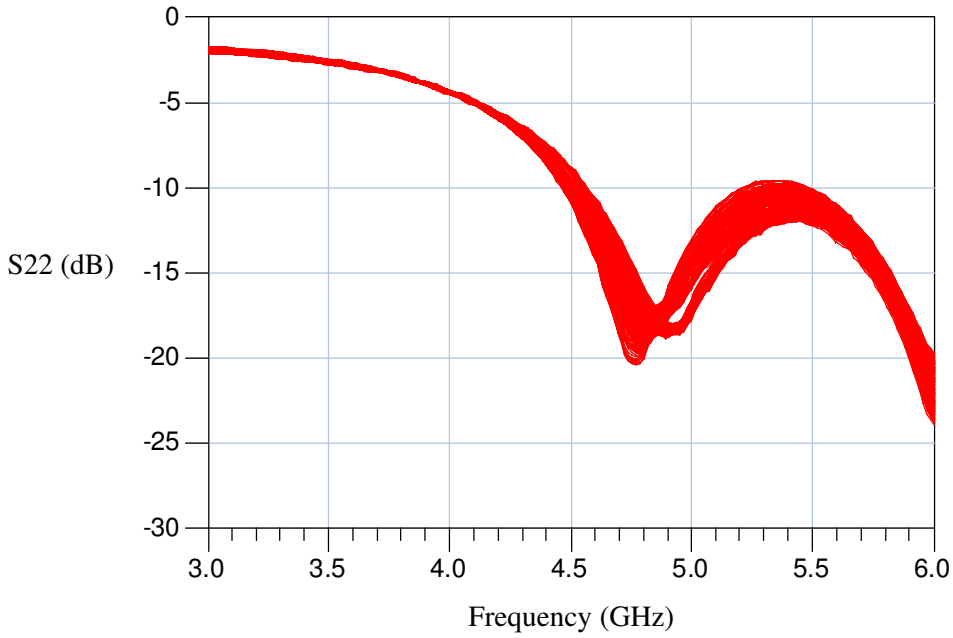


Figure 177: Measured output return loss of the 90º vector modulator phase sifter at various states

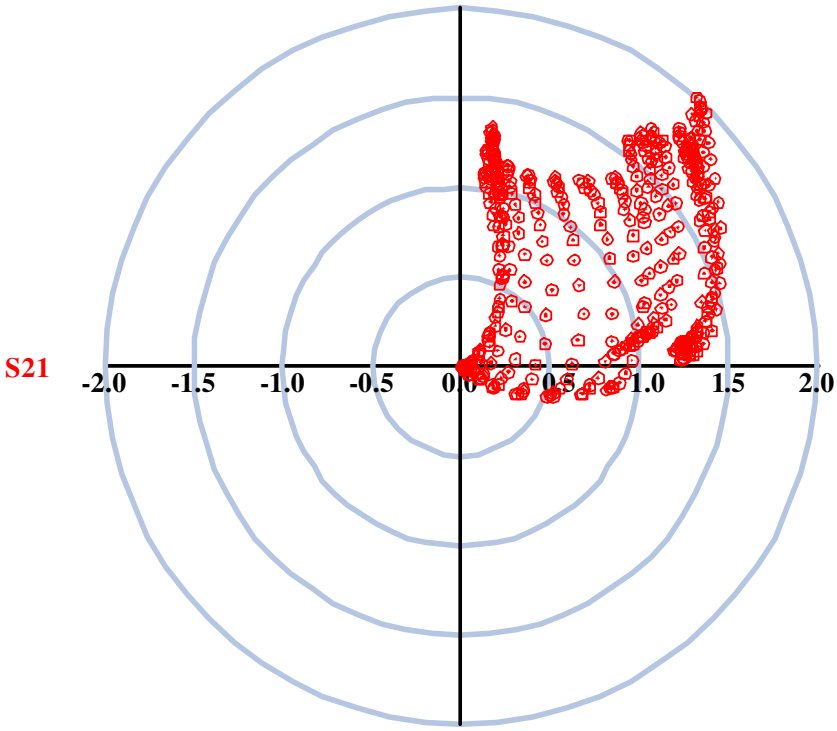


Figure 178: Measured static constellation diagram of the 90º vector modulator phase shifter at 5 GHz with the control voltages of two the VGAs swept from 0.7 to 1V

5.2.4.3 Reflective-Type Phase Shifter (RTPS) Measurements

The fabricated chip was tested using a Cascade Microtech probe station and an Agilent network analyzer. The 150µm G-S-G probes were calibrated with the "Cascade Microtech WinCal" program using an open-short-load-thru (OSLT) calibration method. A photograph of the designed SiGe RTPS is shown in Figure 179.

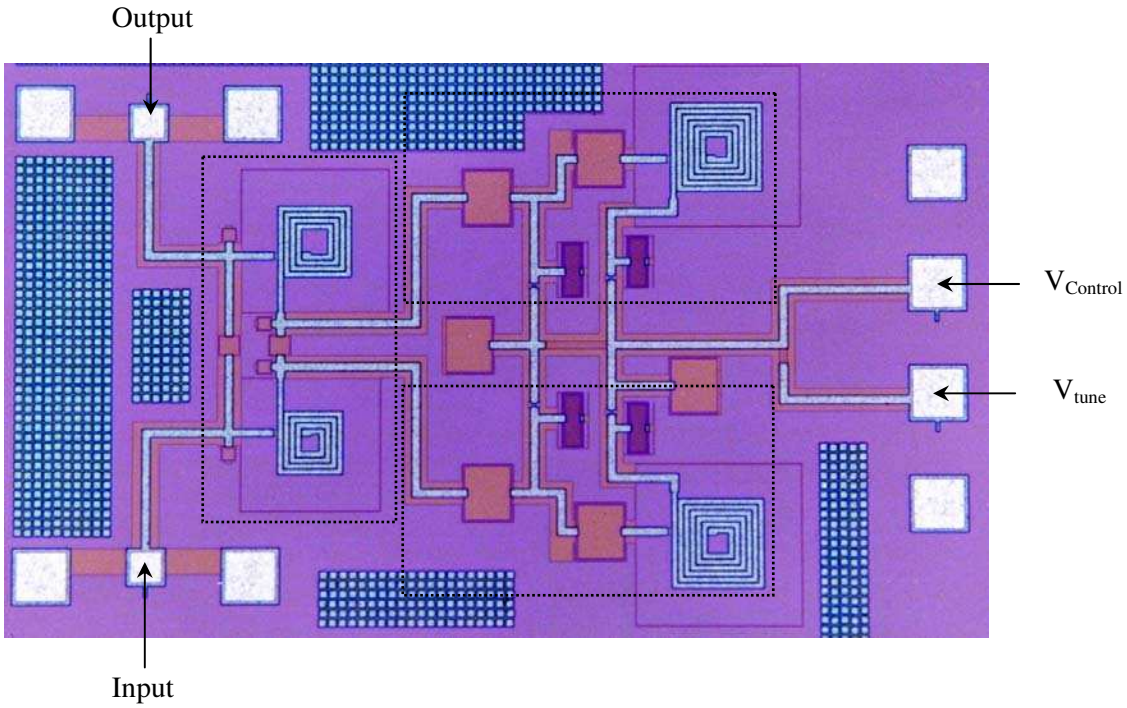


Figure 179: Photograph of the SiGe RTPS including a 90º hybrid coupler (left box) and two TSRL reflective loads (right, upper and lower boxes)

Figure 180 to Figure 182 show the measured relative phase shift, insertion loss, and return loss of the phase shifter with respect to the varactor control voltage, $V_{control}$. The measured maximum relative phase shift is 230° over the 0 – 4V control range. The measured loss over the nominal phase shift range is shown in Figure 181, and it can be seen that the loss varies from -13 dB to -50 dB. Unfortunately this configuration results in large loss variations. For the circuit, the return losses are better than 11 dB. One of the inherent advantages with this RTPS is its excellent return loss performance. The worst-case measured return loss was 11 dB.

Figure 183 shows the measured phase shift of the circuit within a 0.5-GHz bandwidth centered at 4.25 GHz. The measured maximum relative phase shift is larger than 240° at 4.5 GHz.

The insertion loss and return losses of the RTPS phase shifter versus frequency, for various control voltages, are shown in Figure 184 to Figure 186. The worst-case input return loss is 12 dB over the entire range from 4 to 5 GHz, and the worst-case output return loss is 15 dB from 4 to 5 GHz for all states.

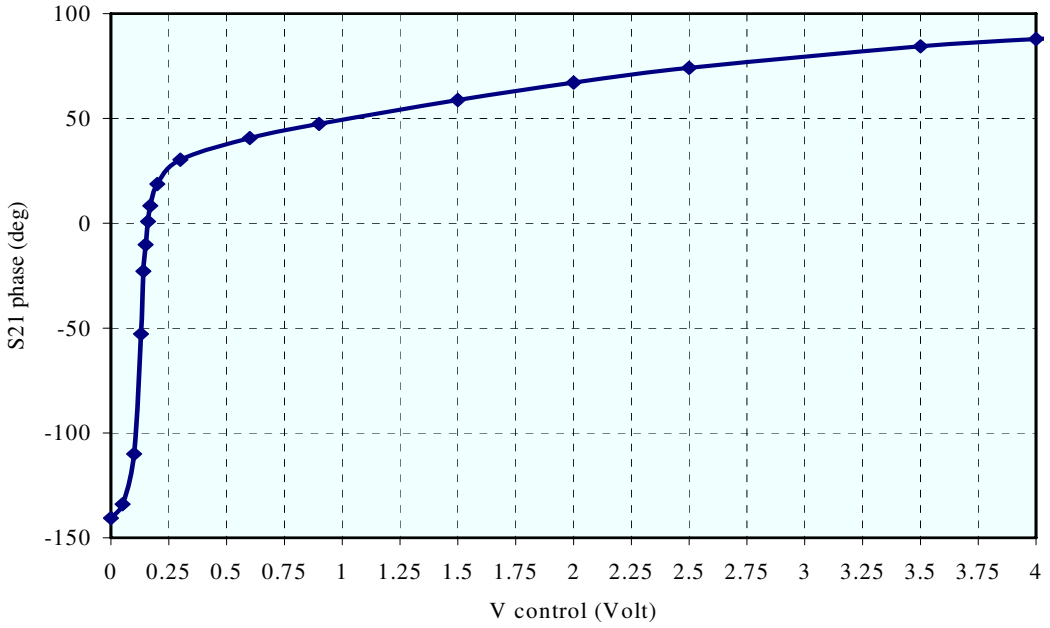


Figure 180: Measured phase shift range of the RTPS versus control voltage

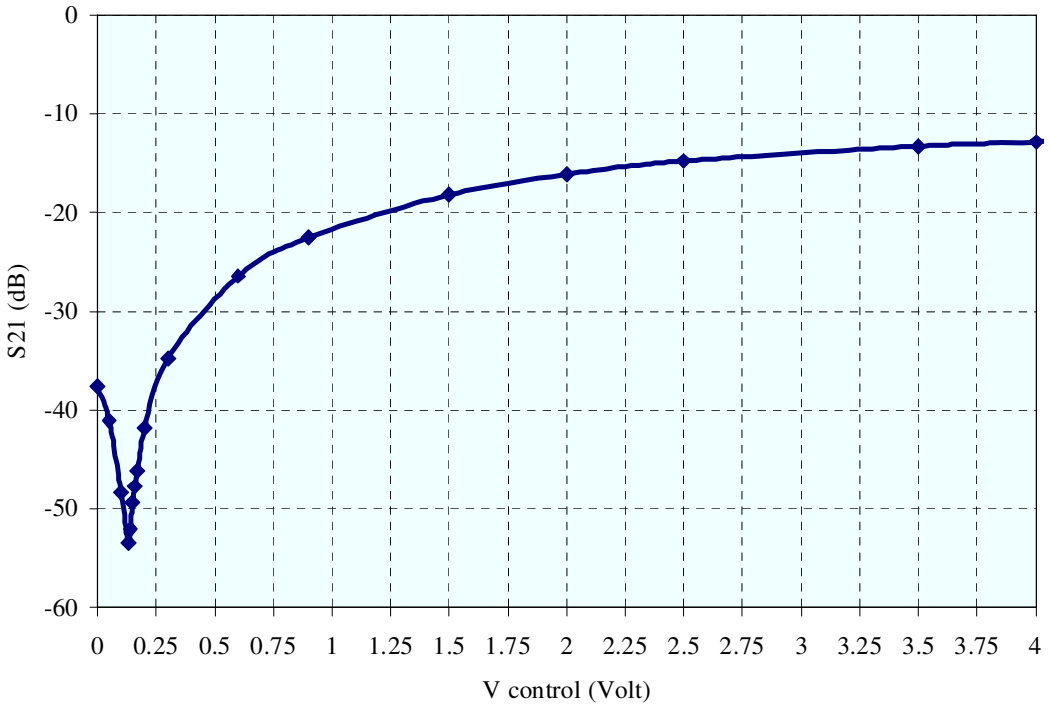


Figure 181: Measured insertion loss of the RTPS versus control voltage

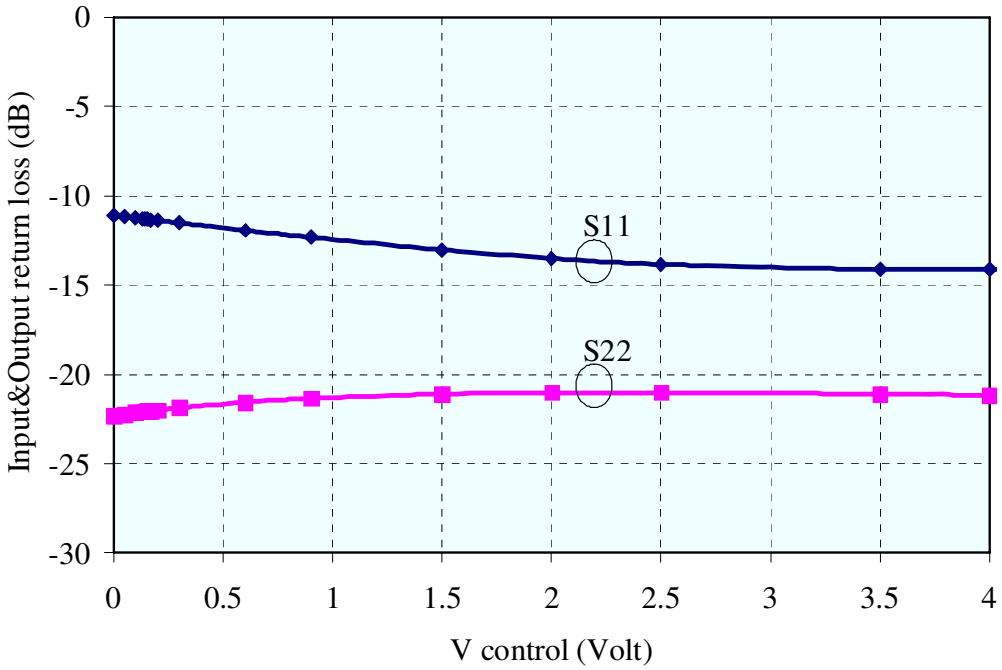


Figure 182: Measured return loss of the RTPS versus control voltage

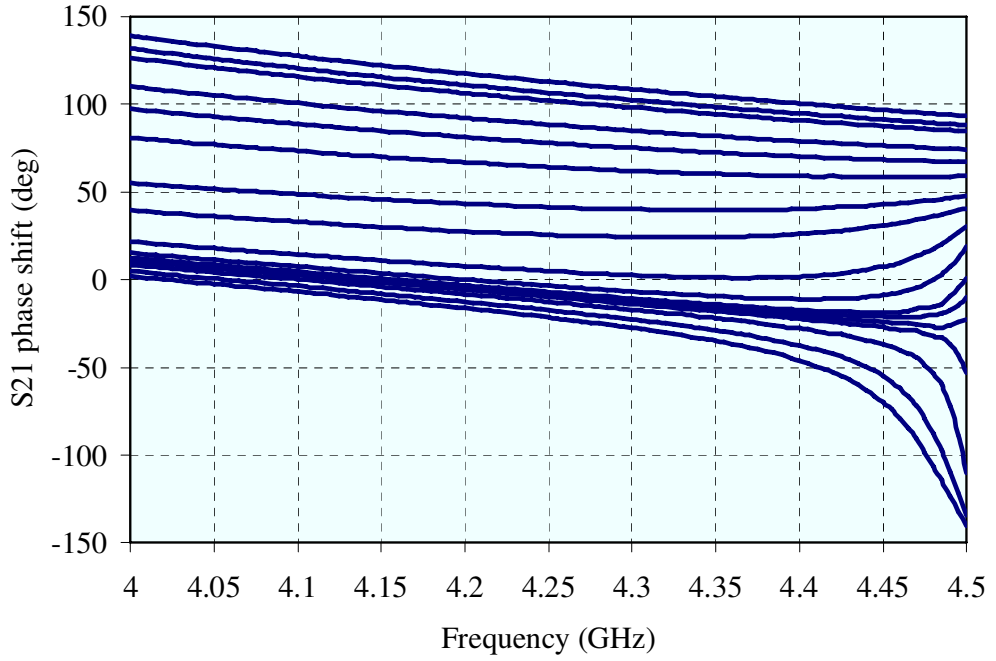


Figure 183: Measured phase shift versus frequency for the same control voltages as in Figure 167

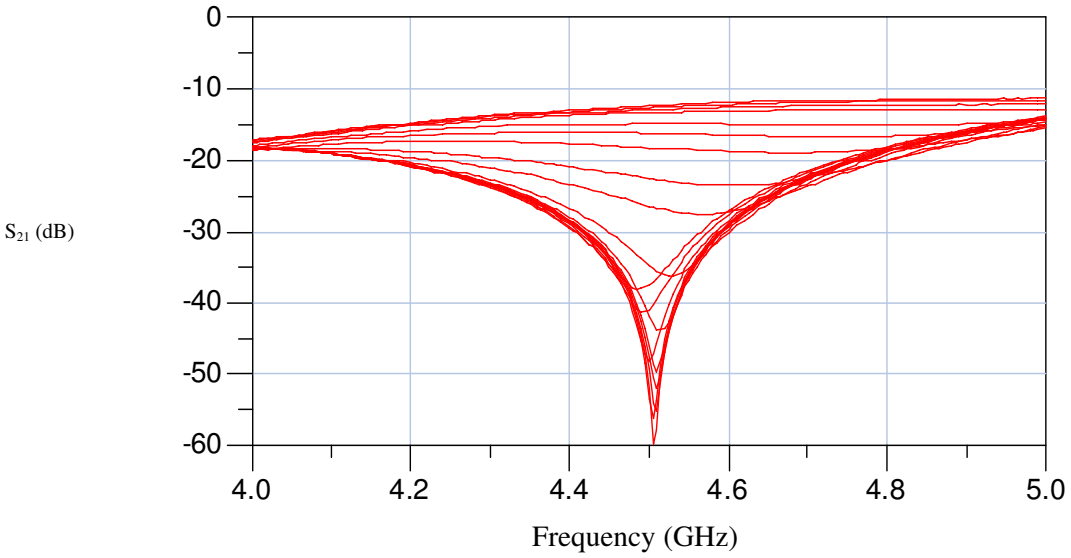


Figure 184: Measured insertion loss versus frequency for different control voltages

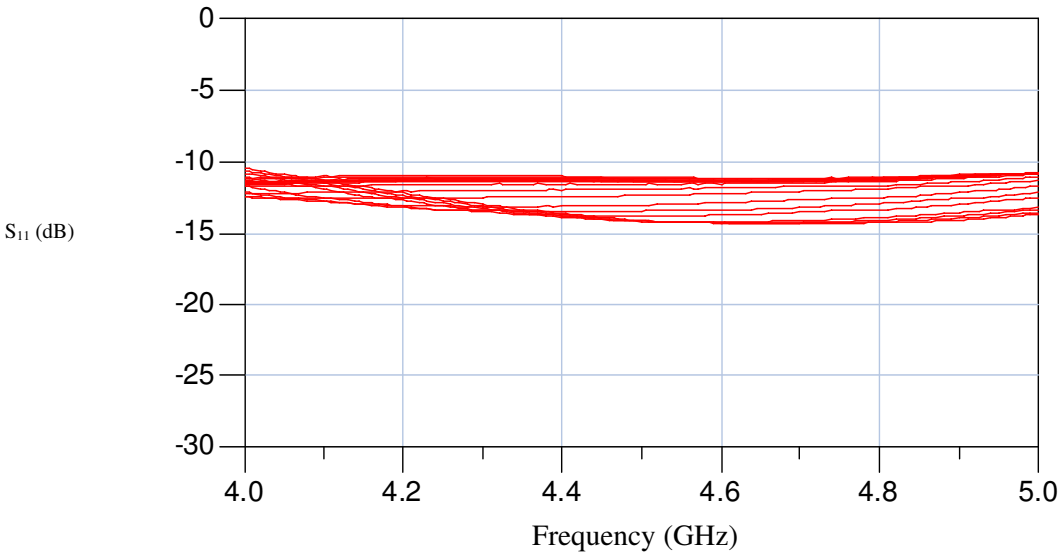


Figure 185: Measured input return loss versus frequency for different control voltages

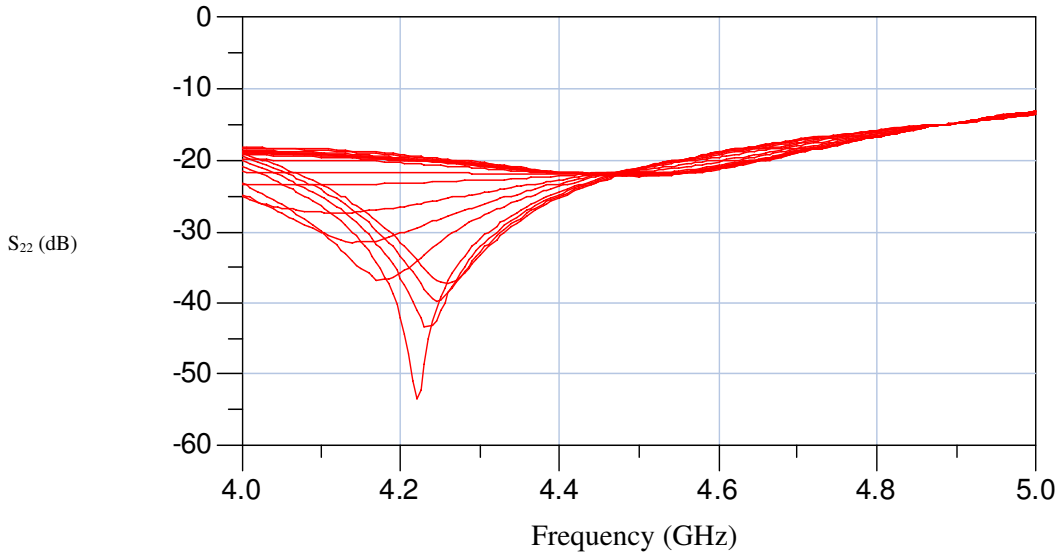


Figure 186: Measured output return loss versus frequency for different control voltages

5.2.4.4 Cascade LNA and Reflective-Type Phase Shifter (RTPS) Measurements

To solve the loss problem of the previous RTPS phase-shifter, a low noise amplifier was cascaded with a RTPS to overcome the high levels of insertion loss, without increasing the risk of instability. A photograph of the designed cascaded LNA and RTPS SiGe is shown in Figure 187.

Figure 188 to Figure 191 show the measured relative phase shift, insertion loss, and return loss of the phase shifter with respect to the varactor control voltage. The measured maximum relative phase shift is 250° over the 0 – 4V control range. The measured insertion loss over the nominal phase shift range is shown in Figure 189, and it can be seen that the loss varies from -4 dB to -38 dB. This configuration improved the loss by about 10 dB. For the circuit, the return losses are better than 16 dB. One of the inherent advantages with this RTPS is its excellent return loss performance. The worst-case measured return loss was 16 dB.

Figure 192 shows the measured phase shift of the circuit within a 0.6 GHz bandwidth centered at 4.3 GHz. The measured maximum relative phase shift is larger than 250° at 4.6 GHz.

The insertion loss and return losses of the cascaded LNA and RTPS phase shifter versus frequency, at various control voltages, is shown in Figure 193 to Figure 195. The worst-case input return loss is 12dB over the entire range from 4 to 5 GHz, and the worst-case output return loss is about 15 dB from 4 to 5 GHz for all states.

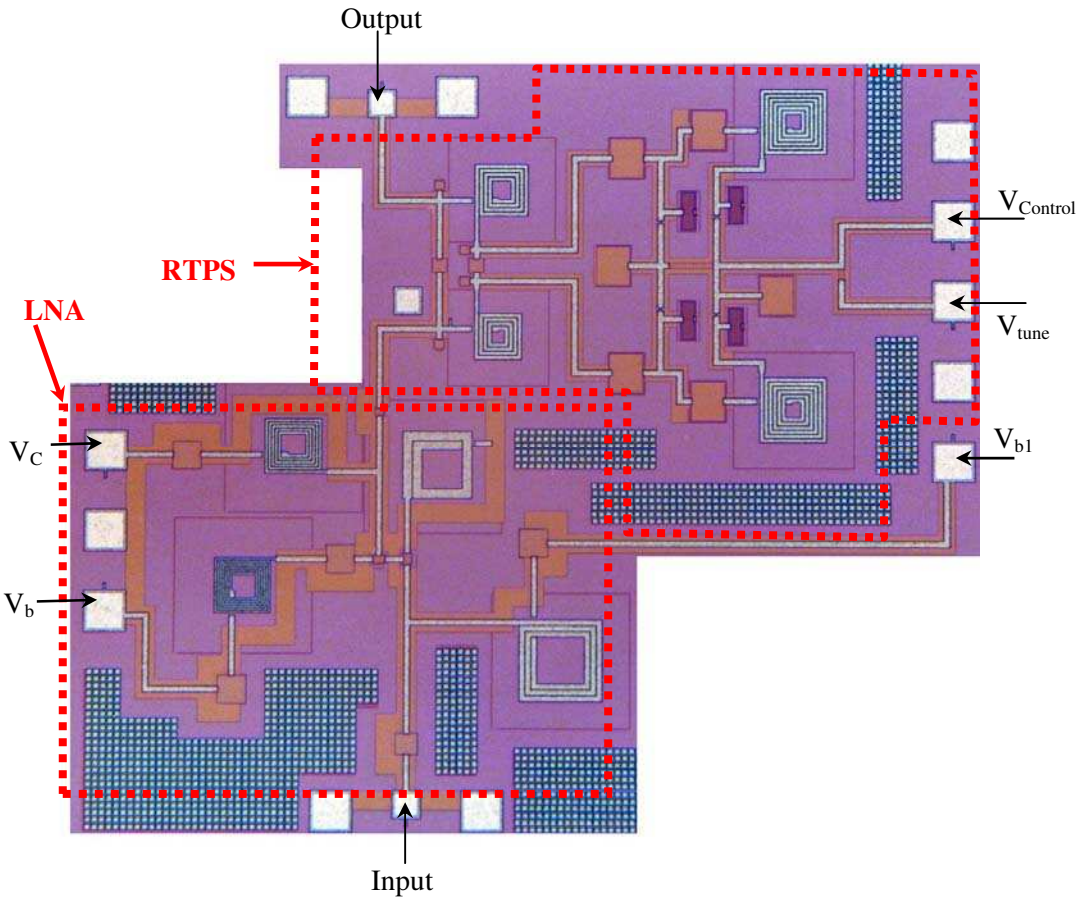


Figure 187: Photograph of the cascaded LNA and RTPS SiGe

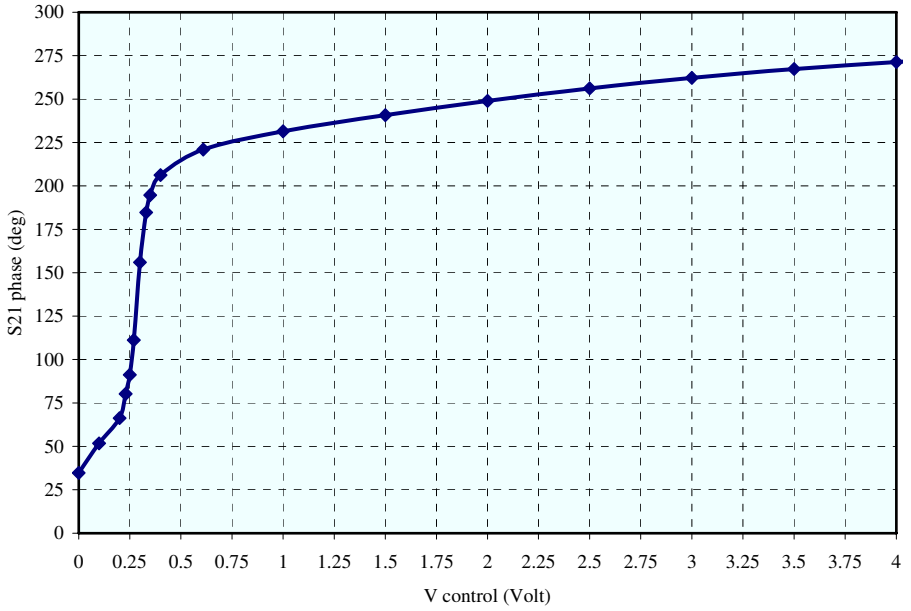


Figure 188: Measured phase shift range of the cascaded LNA and RTPS versus control voltage

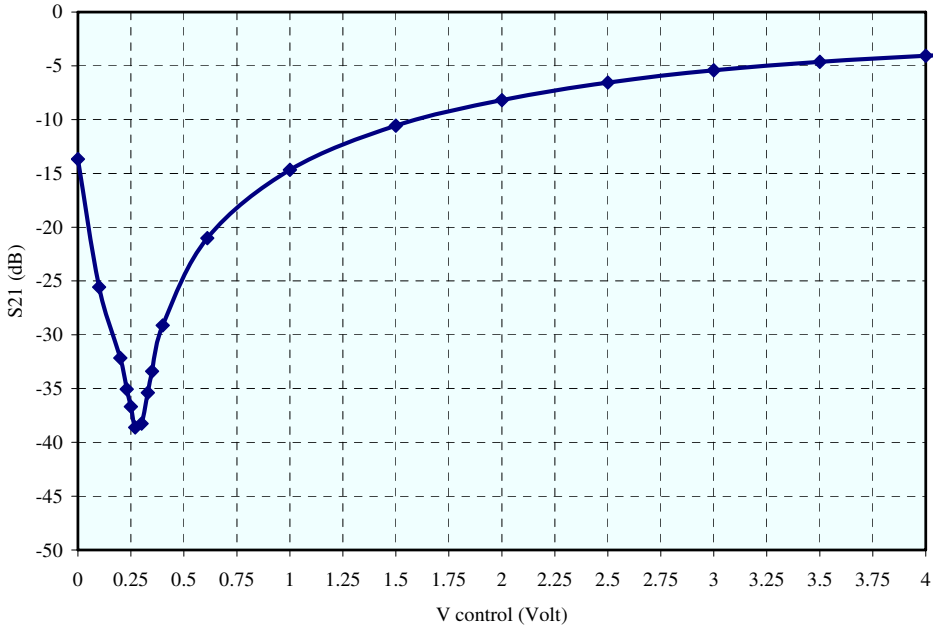


Figure 189: Measured insertion loss of the cascaded LNA and RTPS

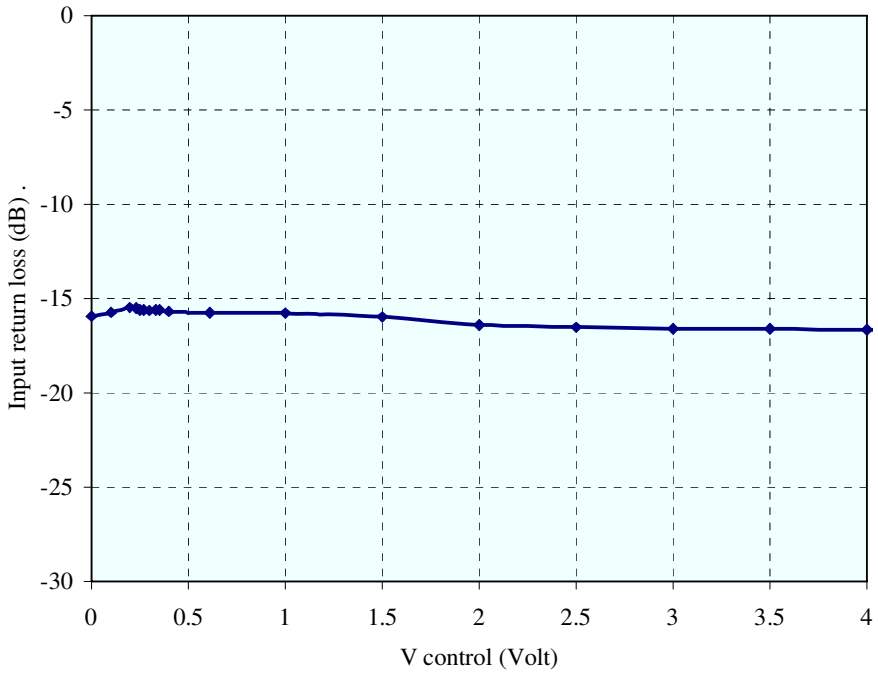


Figure 190: Measured input return loss of the cascaded LNA and RTPS versus control voltage

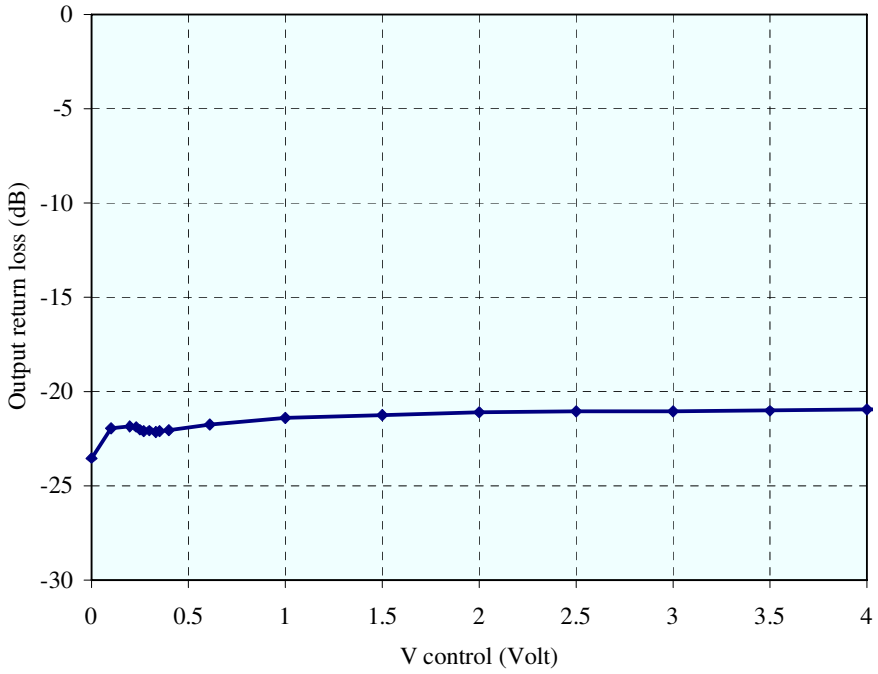


Figure 191: Measured output return loss of the cascaded LNA and RTPS versus control voltage

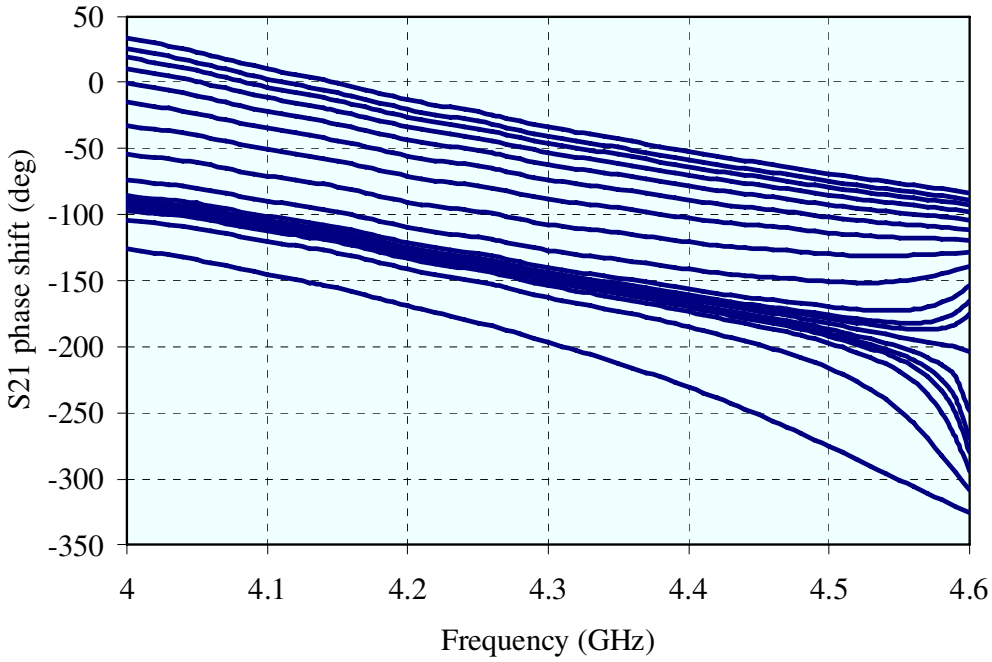


Figure 192: Measured phase shift versus frequency at various control voltages

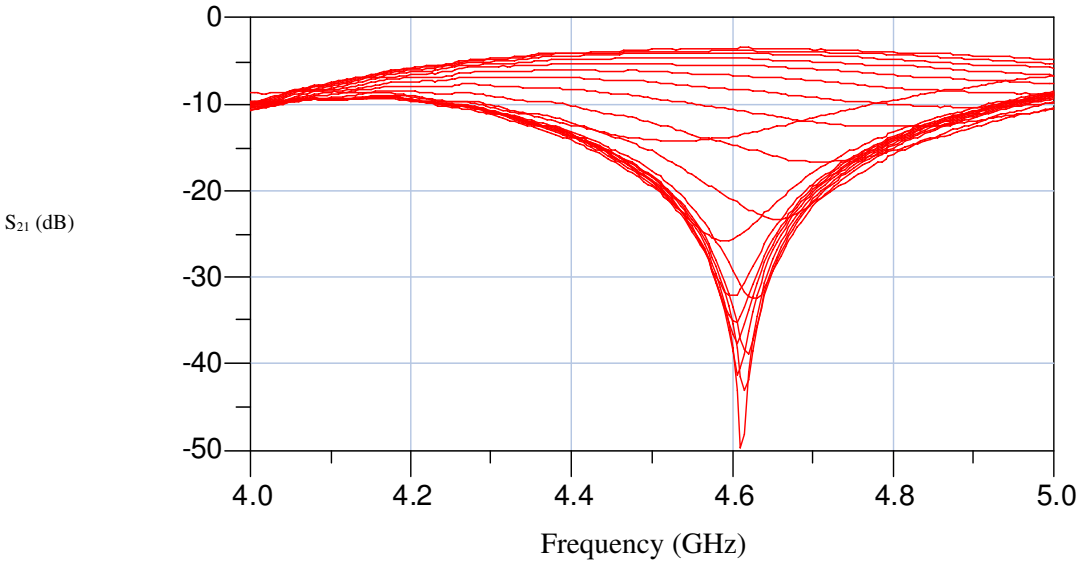


Figure 193: Measured insertion loss versus frequency at various control voltages

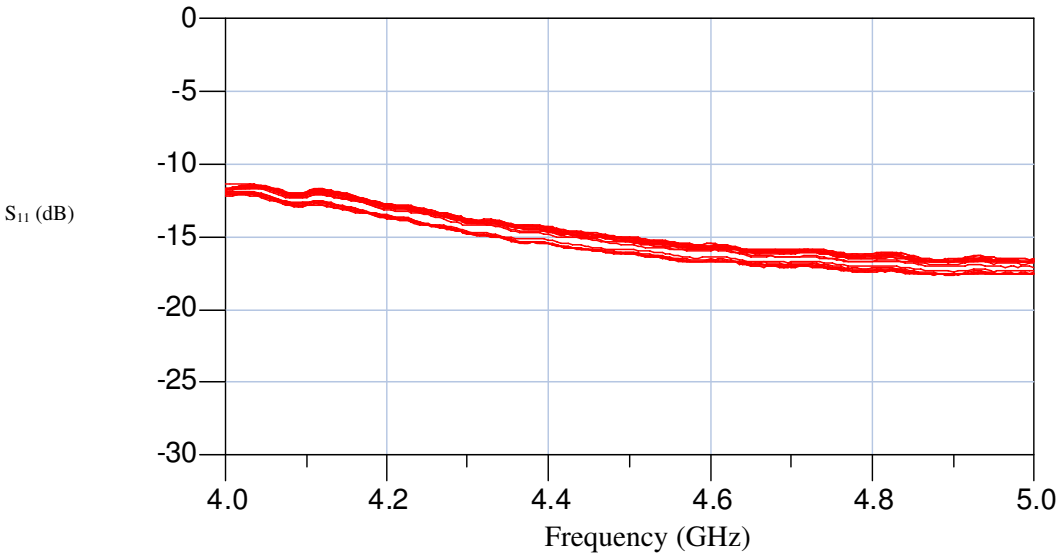


Figure 194: Measured input return loss versus frequency at various control voltages

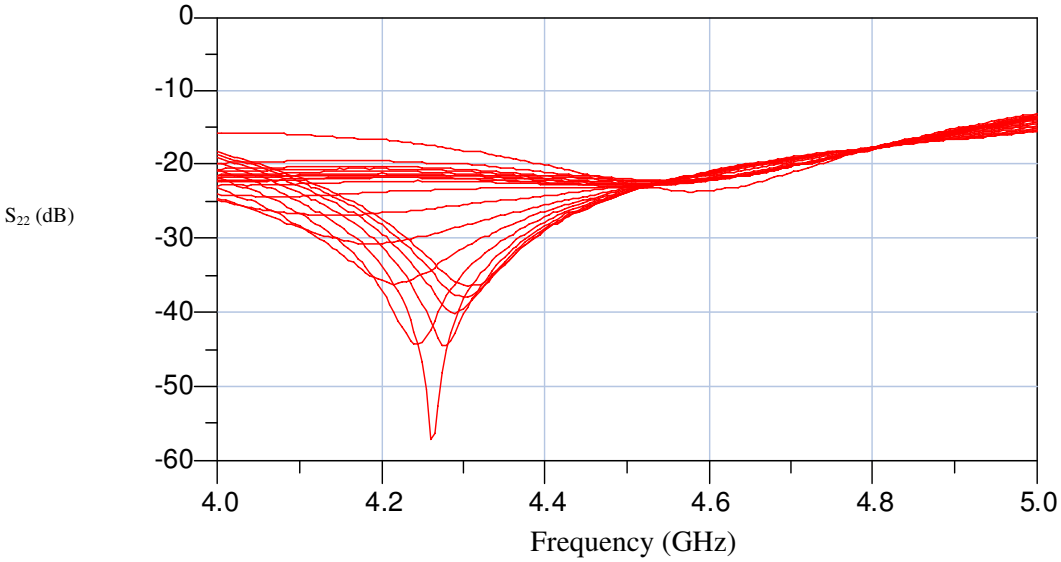


Figure 195: Measured output return loss versus frequency at various control voltages

6 Conclusions

This project investigated silicon RFIC technology for reconfigurable military applications. A design flow was established to successfully design into a 0.35-µm SiGe BiCMOS commercial foundry. Requirements and limitations unique to silicon RFIC technology were explored along with specific RFIC design techniques and circuit topologies. Linear and non-linear RFICs were designed, fabricated and measured to verify these findings. Reconfigurable vector modulators were also demonstrated.

The conclusions resulting from the project may be roughly grouped as follows: silicon RFIC technology, the RFIC design flow and the designed/fabricated RFICs.

Regarding silicon RFIC technology, the project revealed the following key points:

The 0.35-µm SiGe BiCMOS process is well-suited to applications in the 1-10 GHz range; however, for operating frequencies approaching and exceeding 20 GHz it was found to be less suitable.

Thin film microstrip (TFMS) can be effectively used to interconnect circuit elements, although the ground plane width is limited by stress design rules from the foundry. This may cause some loss of the signal due to leakage in the lossy silicon substrate. The small dielectric thickness between the top metal and the bottom metal results in a tightly contained propagating signal which means that circuit elements may be placed quite close to one another resulting in small circuit areas. Furthermore, the availability of multiple metal levels allows for unique distributed structures in RFICs that are not possible using the limited metal layers in traditional GaAs MMICs. Finally, TFMS is easier to layout than conductor-backed coplanar waveguide (which is also commonly used in RFICs) since the uniplanar structures are subject to the maximum width of the stress rule, beyond which any wider geometries require slits.

Metal density requirements are sometimes very difficult to meet, especially when the circuit topologies only make use of the top and bottom metal layers and thus there is very little of the other metal layers in the circuit (thus requiring a large amount of dummy metal fill area which consumes die space). Using arrays of squares is the easiest and most effective way of generating metal fill around the circuits.

Antenna and electro-static discharge (ESD) rules sometimes require diodes to be placed at various places within the circuits, and these diodes may degrade the circuit performance by adding undesired parasitics.

Differential inductors available in the design kit from the foundry proved to be particularly useful to reduce circuit area.

Shielding layers under the inductors were not used; however, they may have improved the circuit performance by increasing the quality factors of the inductors.

Using guard rings around all of the lumped elements was found to improve the circuit performance be reducing undesired element-to-element coupling.

Regarding the design flow for silicon RFICs, the project revealed the following key points:

RFICs can be successfully designed using separate tools for simulation (Agilent ADS) and layout (Mentor Graphics IC Station/Calibre); however, using the layout v. schematic tool to detect errors in the layout is not only important, but *essential* to this design flow.

Schematic-driven layout is *much* less prone to design rule violations and connectivity errors, especially if as many circuit elements as possible are used directly from the foundry design kit (assuming the kit is bug-free, which isn't always the case).

The fabricated RFICs performed well despite not using parasitic extraction available in Mentor Graphics Calibre, and this is likely because TFMS models in Agilent ADS are included in the simulations. Therefore, Calibre parasitic extraction may not be absolutely necessary if ADS interconnect models are used. Future work could include using a planar 3D method of moments solver (such as Agilent Momentum) to see if these simulations can predict the measured performance with even more accuracy.

RFIC circuit performance is highly dependent on the accuracy of the models provided by the foundry (for example, the entire 2005 tape-out was based on models from the foundry that were subsequently found to be inaccurate).

Regarding the designed and fabricated RFICs, the project revealed the following key points:

The lumped cascode LNA topology is very stable and benefits from the fact that most performance metrics can be controlled by individual elements which simplifies the design. The lumped cascode LNA has a measured gain of 11 dB at 5 GHz with an input return loss better than 20 dB and an output return loss better than 13 dB. The measured noise figure is around 3 dB with a measurement uncertainty of about 1 dB.

The measured gain of the distributed LNA was only 0.5 dB at 19 GHz indicating that the 0.35-µm SiGe HBT process may not be suitable for RFIC designs at this frequency.

The cross-coupled VCO topology is capable of generating a very broadband negative resistance, although its performance is limited by the inductor quality factor which is itself limited by the high substrate loss in the silicon. The buffer amplifiers provide a convenient way to match the VCO to 50 Ω without loading the oscillator. The current mirror filter is an effective method to reduce the oscillator phase noise. The measured phase noise at a 1 MHz offset is -112 dBc/Hz. The VCO tuning range is about 4 to 5.5 GHz and the output power at 5.1 GHz is 5 dBm.

Measurements of the 5 GHz active Gilbert Cell mixer demonstrated good performance and excellent linearity for moderate current consumption. The circuit has an input IP3 of -2.5 dBm and a conversion gain of +8.5 dB for an optimum LO power of only 2 dBm.

The 4-bit vector modulator topology can generate 256 different amplitude and phase weight combinations with measured phase shifts from 0º to 360º and measured insertion losses from -13.4 to -32.8 dB at 1.2 GHz. The extra loss of the 180º phase bit causes the states to be less evenly distributed. The input/output return loss is better than 10 dB for all 256 states and the circuit consumes virtually no dc power.

The design and measurement results of a continuous amplitude/phase control SiGe RFIC are presented in this report. This circuit uses the vector sum method to achieve continuous phase and amplitude control. This SiGe circuit is designed for 4.5–5.5 GHz using a 0.35-µm process. Continuous 0-90º phase and 6.8 to -43 dB constant insertion losses can be achieved.

Reactive-type phase shifters (RTPS) have been fabricated in a 0.35-µm SiGe process. The first chip integrates an RTPS with a TSRL network as a load operating at 5 GHz and it achieves a phase shift range greater than 240º. In the second implementation, a RTPS was cascaded with a low noise amplifier to overcome the high levels of insertion loss without increasing the risk of instability. This topology reduces the loss of the complete RTPS by as much as 10 dB while achieving a phase shift range greater than 250º.

This page intentionally left blank.

List of symbols/abbreviations/acronyms/initialisms

A/D	Analog to digital
ADS	Advance design system
$A_{\Delta,RMS}$	RMS amplitude error
A_v	Voltage gain
BE	Base-emitter
BC	Base-collector
bf	Number of base fingers
BiCMOS	Bipolar-CMOS
CAD	Computer-aided design
CB	Common base
CC	Common collector
CE	Common emitter
CPW	Coplanar waveguide
CB-CPW	Conductor-backed coplanar waveguide
CMOS	Complementary metal-oxide semiconductor
CRC	Communications Research Centre Canada
DDS	Direct digital synthesis
DND	Department of National Defence
DRC	Design rule checking
DRDC	Defence Research & Development Canada
DRL	Dual resonated load
DSP	Digital signal processing
el	Emitter width
ERC	Electrical rules checking
ESD	Electrostatic discharge
FET	Field-effect transistor
f_{max}	Maximum frequency of oscillation
f_T	Transit frequency
Γ	Reflection coefficient
gdsii	Graphic data system II

GPS	Global positioning system
GPPG	Ground-power-power-ground
GSG	Ground-signal-ground
HB	Harmonic balance
HBT	Hetrojunction bipolar transistor
HP/LP	High-pass/low-pass
IC	Integrated circuit
IF	Intermediate frequency
IIP3	Input third-order intercept point
IL	Insertion loss
IM3	Third-order intermodulation
I_{tail}	Tail current
K	Stability factor
LC	Inductor-capacitor
L_d	Varactor finger length
LNA	Low noise amplifier
LO	Local oscillator
LPF	Low-pass filter
LSSP	Large-signal s-parameter
LUP	Latch-up
LVS	Layout versus schematic
MAG	Maximum available gain
MEMS	Microelectromechanical systems
MMIC	Monolithic microwave integrated circuit
N_a	Number of varactor fingers
NF	Noise figure
OSLT	Open-short-load-thru
P_{1dB}	1-dB compression point
Q	Quality factor
RF	Radio frequency
RFIC	Radio frequency integrated circuit
RL	Return loss

R_L	Load resistance
RTPS	Reflective-type phase shifter
SiGe	Silicon Germanium
SRF	Self-resonant frequency
SRL	Single resonated load
SPDT	Single-pole double-throw
SSA	Signal-source analyzer
SSB	Single side band
SSLG	Small-signal loop gain
$\theta_{\Delta,RMS}$	RMS phase error
TFMS	Thin film microstrip
T/R	Transmit/receive
TSRL	Transformed single resonated load
VCO	Voltage controlled oscillator
VGA	Variable gain amplifier
VNA	Vector network analyzer
V_{tune}	Tuning voltage
	Angular frequency
W_d	Varactor finger width
Z_{in}	Input impedance
Z_o	Characteristic impedance
Z_{out}	Output impedance

DOCUMENT CONTROL DATA

(Security classification of title, body of abstract and indexing annotation must be entered when the overall document is classified)

1. ORIGINATOR (The name and address of the organization preparing the document. Organizations for whom the document was prepared, e.g. Centre sponsoring a contractor's report, or tasking agency, are entered in section 8.)

Defence R&D Canada – Ottawa
3701 Carling Avenue
Ottawa, Ontario K1A 0Z4

2. SECURITY CLASSIFICATION (Overall security classification of the document including special warning terms if applicable.)

UNCLASSIFIED

3. TITLE (The complete document title as indicated on the title page. Its classification should be indicated by the appropriate abbreviation (S, C or U) in parentheses after the title.)

Silicon RFIC techniques for reconfigurable military applications

4. AUTHORS (last name, followed by initials – ranks, titles, etc. not to be used)

McLelland, S. R.; Hettak, K.; Glaser, C.; DesOrmeaux, L.; Morin, G. A.

5. DATE OF PUBLICATION (Month and year of publication of document.)

December 2008

6a. NO. OF PAGES (Total containing information, including Annexes, Appendices, etc.)

169

6b. NO. OF REFS (Total cited in document.)

0

7. DESCRIPTIVE NOTES (The category of the document, e.g. technical report, technical note or memorandum. If appropriate, enter the type of report, e.g. interim, progress, summary, annual or final. Give the inclusive dates when a specific reporting period is covered.)

Technical Report

8. SPONSORING ACTIVITY (The name of the department project office or laboratory sponsoring the research and development – include address.)

Defence R&D Canada – Ottawa
3701 Carling Avenue
Ottawa, Ontario K1A 0Z4

9a. PROJECT OR GRANT NO. (If appropriate, the applicable research and development project or grant number under which the document was written. Please specify whether project or grant.)

9b. CONTRACT NO. (If appropriate, the applicable number under which the document was written.)

10a. ORIGINATOR'S DOCUMENT NUMBER (The official document number by which the document is identified by the originating activity. This number must be unique to this document.)

DRDC Ottawa TR 2008-295

10b. OTHER DOCUMENT NO(s). (Any other numbers which may be assigned this document either by the originator or by the sponsor.)

11. DOCUMENT AVAILABILITY (Any limitations on further dissemination of the document, other than those imposed by security classification.)

Unlimited

12. DOCUMENT ANNOUNCEMENT (Any limitation to the bibliographic announcement of this document. This will normally correspond to the Document Availability (11). However, where further distribution (beyond the audience specified in (11) is possible, a wider announcement audience may be selected.))

Unlimited

13. ABSTRACT (A brief and factual summary of the document. It may also appear elsewhere in the body of the document itself. It is highly desirable that the abstract of classified documents be unclassified. Each paragraph of the abstract shall begin with an indication of the security classification of the information in the paragraph (unless the document itself is unclassified) represented as (S), (C), (R), or (U). It is not necessary to include here abstracts in both official languages unless the text is bilingual.)

The functionality of silicon radio frequency integrated circuits (RFICs) makes the technology particularly suitable for reconfigurable circuits. Designing silicon RFICs requires expertise in the design, simulation and verification of traditional monolithic microwave integrated circuits (MMICs) while also considering a number of requirements unique to silicon RFIC technology. This report shows how MMIC and RFIC design techniques can be combined to yield high performance circuits and a comprehensive design flow for silicon RFICs. This RFIC design flow was validated by designing both linear and nonlinear circuits that were fabricated using a commercial 0.35-µm SiGe BiCMOS process. These circuits include low noise amplifiers, a voltage controlled oscillator, a double-balanced mixer, a reflection type phase shifter, an analog vector modulator and a 4-bit vector modulator. The two vector modulators generate the variable amplitude and phase weights needed for adaptive phase arrays, which have been proposed to improve the anti-jamming performance of military GPS units.

La fonctionnalité des circuits intégrés de radiofréquence en silicium (RFICs) rende la technologie particulièrement appropriée aux circuits re-configurables. Concevoir des RFICs en silicium exige l'expertise dans la conception, la simulation et la vérification des circuits intégrés monolithiques hyperfréquences (MMICs) traditionnels tout en considérant également un certain nombre de conditions uniques à la technologie du RFIC en silicium. Ce rapport met en évidence comment des techniques de conception en MMIC et en RFIC peuvent être conjugués pour générer des circuits a haut rendement et un processus de conception compréhensive pour le RFICs en silicium. Cet processus de conception de RFIC a été validé en concevant les circuits linéaires et non-linéaires qui ont été fabriqués en utilisant un processus commercial 0.35-µm SiGe BiCMOS. Ces circuits incluent des amplificateurs à faible bruit, un oscillateur commandé par une source de tension, un mélangeur double-équilibré, un déphaseur à réflexion, un modulateur vectoriel analog et un modulateur vectoriel à 4 bits. Les deux modulateurs vectoriels produisent des poids variables en amplitude et en phase requis pour les réseaux phasés adaptatifs, qui ont été proposées pour améliorer la performance antibrouillage des unités GPS militaires.

14. KEYWORDS, DESCRIPTORS or IDENTIFIERS (Technically meaningful terms or short phrases that characterize a document and could be helpful in cataloguing the document. They should be selected so that no security classification is required. Identifiers, such as equipment model designation, trade name, military project code name, geographic location may also be included. If possible keywords should be selected from a published thesaurus, e.g. Thesaurus of Engineering and Scientific Terms (TEST) and that thesaurus identified. If it is not possible to select indexing terms which are Unclassified, the classification of each should be indicated as with the title.)

Radio frequency integrated circuits; Silicon gemanium BiCMOS; Adaptive phased arrays; LNA; VCO; Gilbert cell mixer; Vector modulator

Defence R&D Canada

Canada's leader in Defence
and National Security
Science and Technology

R & D pour la défense Canada

Chef de file au Canada en matière
de science et de technologie pour
la défense et la sécurité nationale

www.drdc-rddc.gc.ca